PRODUCT SPECIFICATION

4.0" TFT LCD MODULE
MODEL: YDP LCD I S 400 MI

< ◇ >   Preliminary Specification

< ◆ >   Finally Specification

CUSTOMER'S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY
-	TFT S.G.H 20240530	TFT 周福云 20240530	TFT L.L 20240530

knitter-switch

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2022.08.23	ZYJ	Initial Release	
1.1	2022.08.29	ZYJ	Modify Interface Pins Definition Modify Outline Drawing	P10 P30
1.2	2024.05.30	LL	Modify Driver IC Modify Absolute Maximum Ratings Modify DC Characteristics Modify AC characteristics Modify Outline Drawing(B)	P4 P4 P5 P11-15 P30

Table of Contents

1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	4.0"	
LCD type	IPS TFT	
Display Mode	Transmissive /Normal Black	
Resolution	720 RGB x 720	Pixels
View Direction	Full viewing	Best Image
Module Outline	75.326(H) x 79.522(V) x 2.9(T) (Note1)	mm
Active Area	71.928(H) x 71.928(V)	mm
Pixel Pitch	99.9(H) x 99.9(V)	um
Pixel Arrangement	RGB Vertical stripe	
Display Colors	16.7M	
Interface	MIPI	
Driver IC	JD9365DA-H3	
With or without the touch panel	Without	
Operating Temperature	**-20～70**	℃
Storage Temperature	**-30～80**	℃
Weight	(31)	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

GND=0V, Ta=25℃

Item	Symbol	Min.	Max.	Unit
Supply Voltage	VCI	-0.3	6.6	V
	IOVCC	-0.3	3.6	V
Storage temperature	T_{STG}	**-30**	**+80**	℃
Operating temperature	T_{OP}	**-20**	**+70**	℃

Note 1: If Ta below 50℃, the maximal humidity is 90%RH, if Ta over 50℃, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCI	2.5	-	6.0	V
	IOVCC	1.65	-	3.6	V
Logic Low input voltage	V_{IL}	GND	-	0.3*IOVCC	V
Logic High input voltage	V_{IH}	0.7*IOVCC	-	IOVCC	V
Logic Low output voltage	V_{OL}	GND	-	0.2*IOVCC	V
Logic High output voltage	V_{OH}	0.8*IOVCC	-	IOVCC	V
Current Consumption All White	Ivcc	-	(17)	-	mA

5. Backlight Characteristic

5.1. Backlight Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V_F	Ta=25 ℃, I_F=20mA/LED	12	**12.8**	13.6	V
Forward Current	I_F	Ta=25 ℃, V_F=3.2V/LED	-	**40**	-	mA
Power dissipation	P_D	-	-	**512**	-	mW
Uniformity	Avg	-	80	-	-	%
LED working life(25℃)			-	30000	-	Hrs
Drive method	Constant current					
LED Configuration	8 White LEDs (4 LEDs in one string and 2 groups in parallel)					

Note1: LED life time defined as follows: The final brightness is at 50% of original brightness.

The environmental conducted under ambient air flow, at Ta=25±2 ℃,60%RH±5%, I_F=20mA/LED.

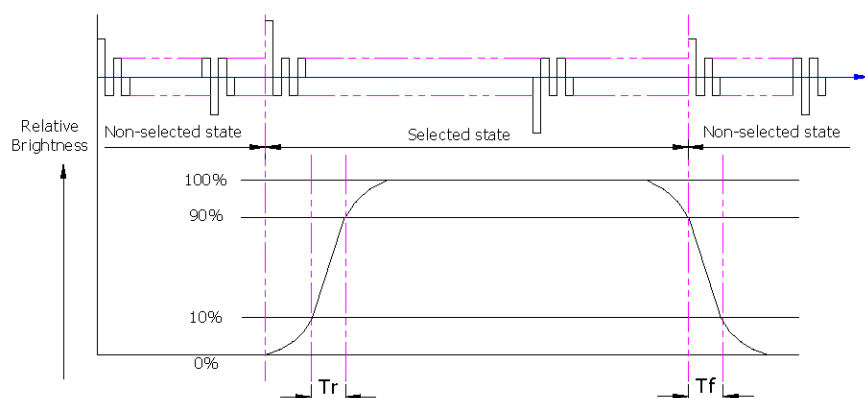### 5.2. Backlighting circuit
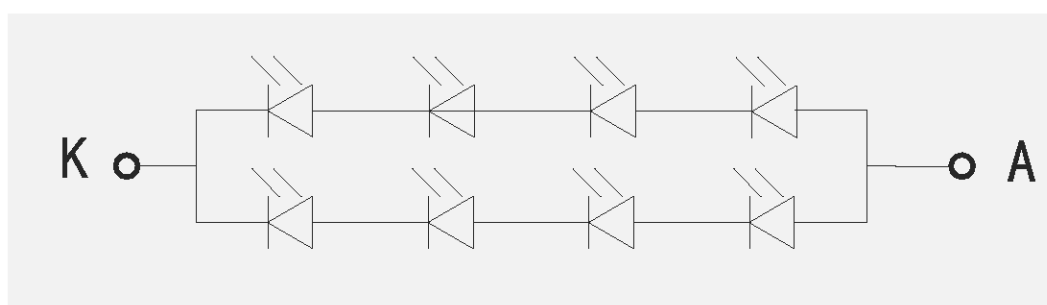
6. Optical Characteristics

6.1. Optical Characteristics

Ta=25ºC, VCI=2.8V, IOVCC=1.8V

Item		Symbol	Condition	Specification			Unit
				Min.	Typ.	Max.	
Luminance on TFT(I_f=20mA/LED)		Lv	Normally viewing angle θx = φY =0º	296	370	-	cd/m²
Contrast ratio(See 6.3)		CR		900	1200	-	
Response time (See 6.2)		TR+TF		-	30	40	ms
Chromaticity Transmissive (See6.5)	Red	XR		0.595	0.645	0.695	
		YR		0.268	0.318	0.368	
	Green	XG		0.245	0.295	0.345	
		YG		0.554	0.604	0.654	
	Blue	XB		0.083	0.133	0.183	
		YB		0.016	0.066	0.116	
	White	Xw		0.234	0.284	0.334	
		Yw		0.275	0.325	0.375	
Viewing Angle (See 6.4)	Horizontal	θx+	Center CR≥10	80	85	-	Deg.
		θx-		80	85	-	
	Vertical	φY+		80	85	-	
		φY-		80	85	-	
NTSC Ratio(Gamut)				63	68	-	%

(Leftmost column spanning all rows: **Backlight On (Transmissive Mode)**)

6.2. Definition of Response Time

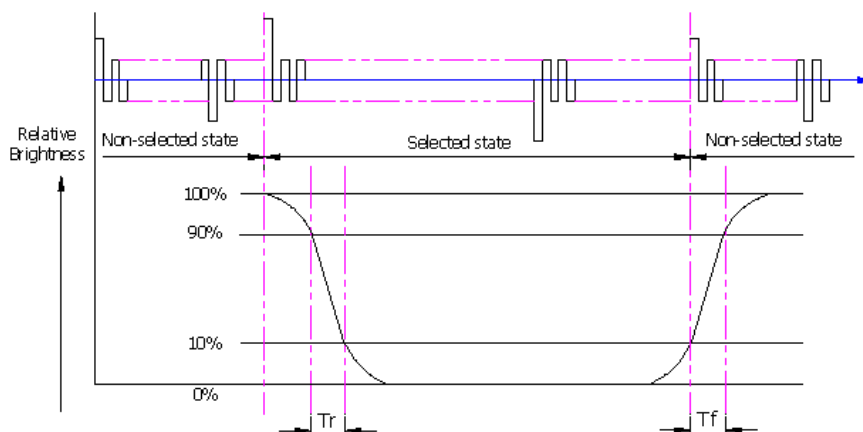#### 6.2.1. Normally Black Type (Negative)

Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note: Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)

Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

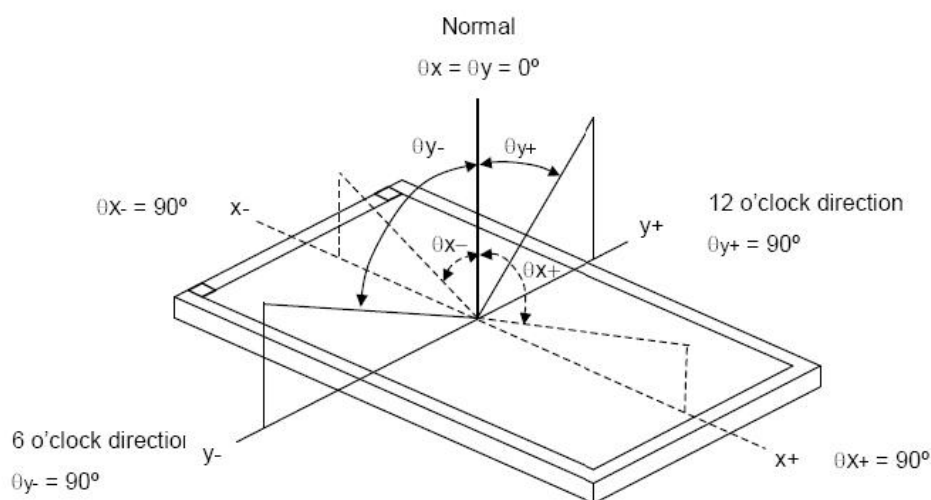Note: Measuring machine: LCD-5100 or EQUI

6.3. Definition of Contrast Ratio

Contrast is measured perpendicular to display surface in reflective and transmissive mode. The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel
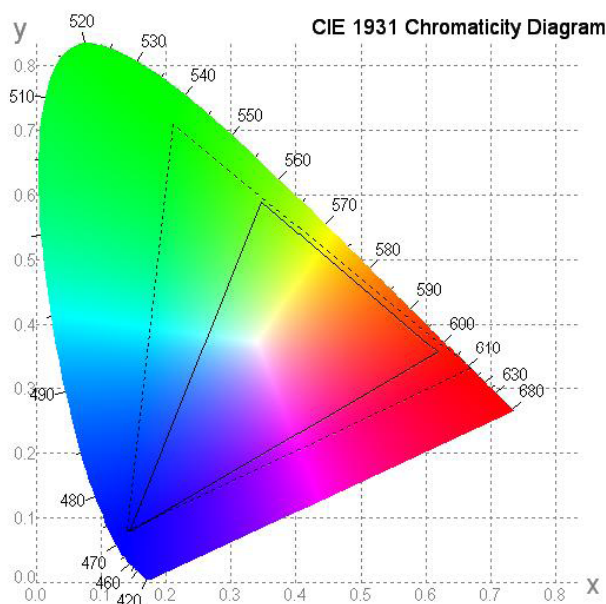
6.4. Definition of Viewing Angles

Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)

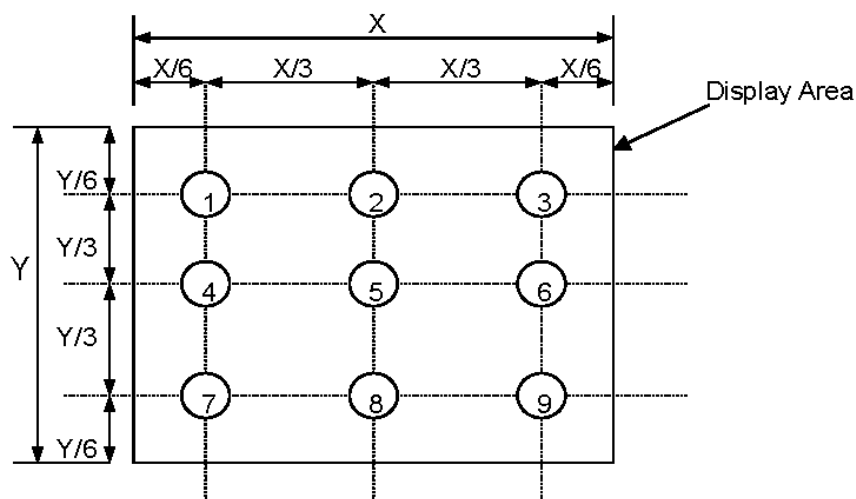## 6.6. Definition of Surface Luminance, Uniformity and Transmittance

Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1.   Surface Luminance: L_V = average (L_{P1}:L_{P9})

6.6.2.   Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%
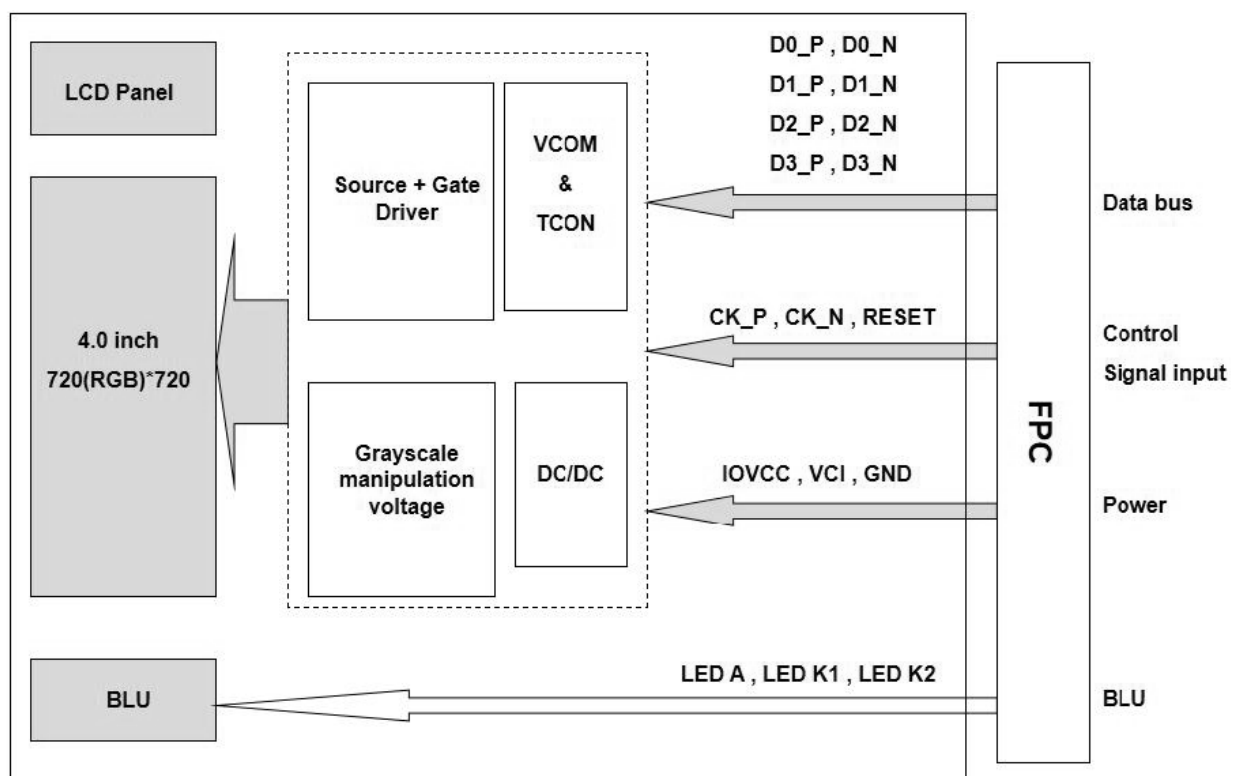
6.6.3.   Transmittance = L_V on LCD / L_V on Backlight * 100%

Note: Measuring machine: BM-7

7. Block Diagram and Power Supply

8. Interface Pins Definition

No.	Symbol	Function	Remark
1	LED K	LED cathode.	
2	LED A1	LED anode.	
3	LED A2	LED anode.	
4	VCI	Power supply to the analog circuit.(2.8V)	
5	IOVCC	Power supply for the logic power and I/O circuit.(1.8V)	
6	RESET	Global reset pin.	
7	TE	Tearing Effect pin.No connect.	
8	PWM	No connect.	
9	GND	Ground.	
10	D0_P	MIPI positive data signal.(+)	
11	D0_N	MIPI negative data signal.(-)	
12	GND	Ground.	
13	D1_P	MIPI positive data signal.(+)	
14	D1_N	MIPI negative data signal.(-)	
15	GND	Ground.	
16	CK_P	MIPI positive clock signal.(+)	
17	CK_N	MIPI negative clock signal.(-)	
18	GND	Ground.	
19	D2_P	MIPI positive data signal.(+)	
20	D2_N	MIPI negative data signal.(-)	
21	GND	Ground.	
22	D3_P	MIPI positive data signal.(+)	
23	D3_N	MIPI negative data signal.(-)	
24	GND	Ground.	
25	NC(TP_INT)	No connect.	
26	NC(TP_SDA)	No connect.	
27	NC(TP_SCL)	No connect.	
28	NC(TP_RST)	No connect.	
29	NC(TP_VCI)	No connect.	
30	NC(TP_IOVCC)	No connect.	

9. AC characteristics

9.1. The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

2) The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 13.4 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.
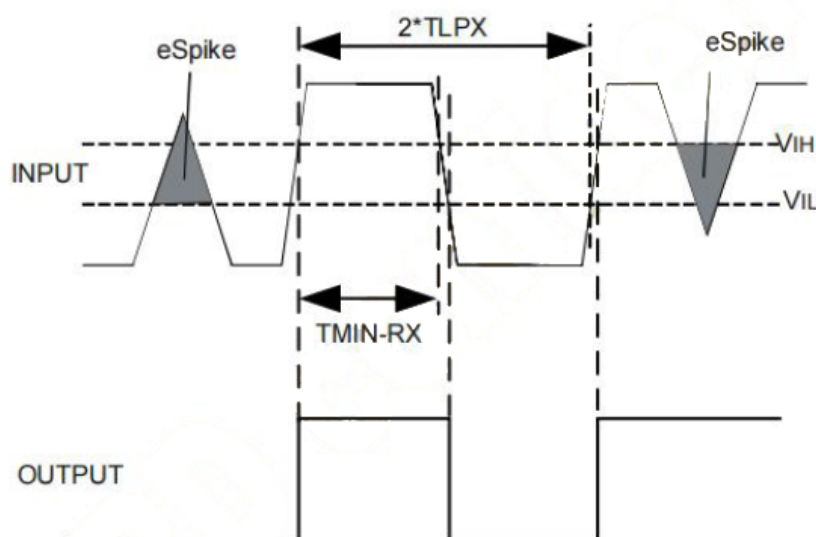
Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

3) High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

4) High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.
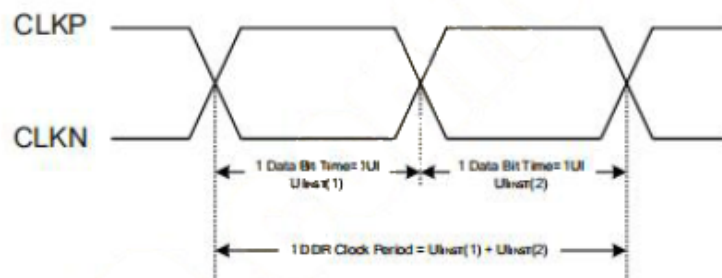
The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

9.2. RGB timing table

TBD

9.3. reset input timing
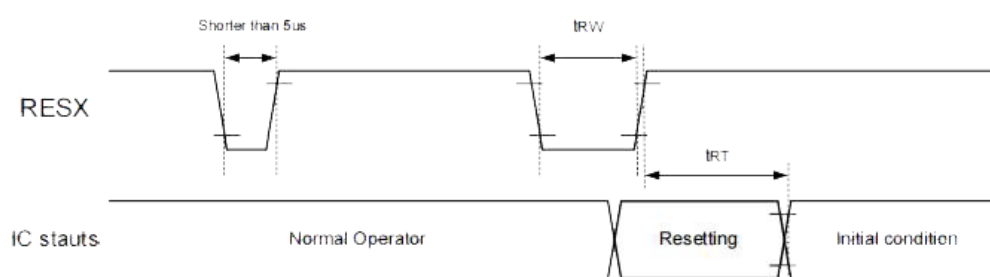
Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width[2]	RESX	10	-	µs
t_{RT}	Reset complete time[3]	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:

10µs

Reset is accepted

10µs

20ns Less than 20ns width positive spike will be rejected.
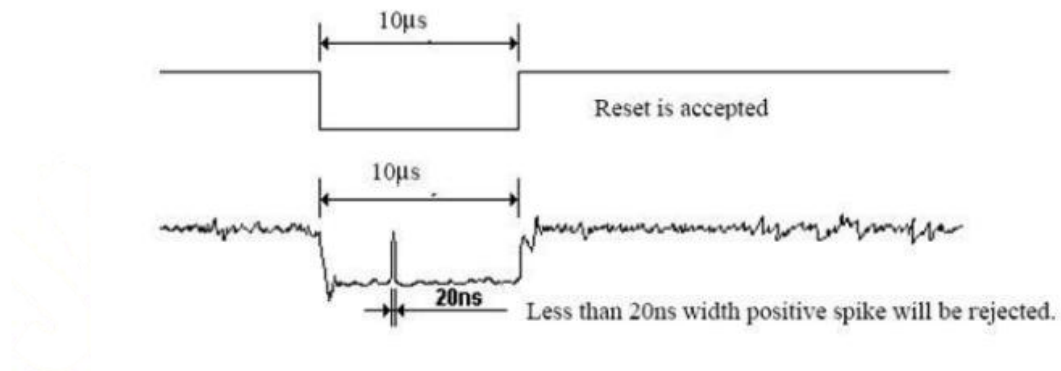
(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.
(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

10. Quality Assurance

10.1. Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

10.2. Standard for Quality Test

10.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

10.2.2. Sampling Criteria:

Visual inspection: AQL 1.5

Electrical functional: AQL 0.65.

10.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

10.3. Nonconforming Analysis & Disposition

10.3.1. Nonconforming analysis:

10.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

10.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

10.3.1.3. If can not finish the analysis on time, customer will be notified with the progress status.

10.3.2. Disposition of nonconforming:

10.3.2.1. Non-conforming product over PPM level will be replaced.

10.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

10.4. Agreement Items

Shall negotiate with customer if the following situation occurs:

10.4.1. There is any discrepancy in standard of quality assurance.

10.4.2. Additional requirement to be added in product specification.

10.4.3. Any other special problem.

10.5. Standard of the Product Visual Inspection

10.5.1. Appearance inspection:

10.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

10.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

10.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,
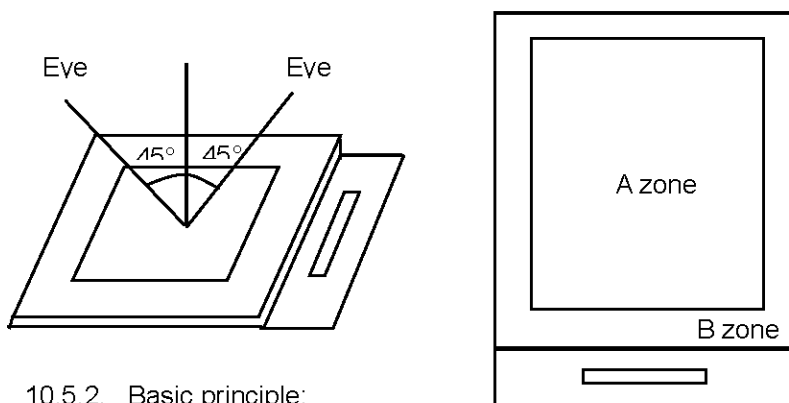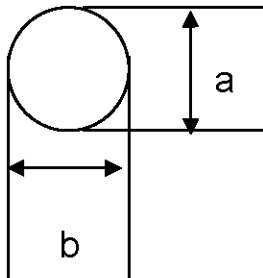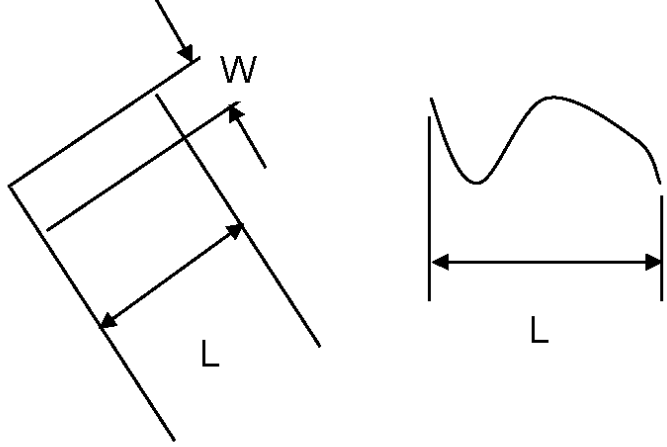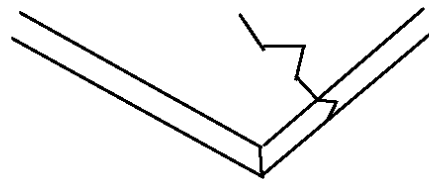
10.5.2. Basic principle:
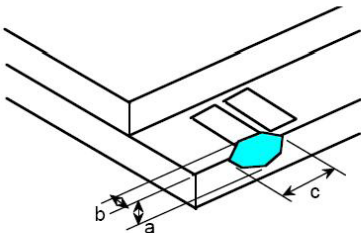
10.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

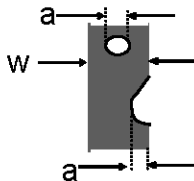10.5.2.2. New item must be added on time when it is necessary.

10.6. Inspection Specification

No.	Item	Criteria (Unit: mm)
01	Black / White spot Foreign material (Round type) Pinholes Stain Particles inside cell. (Minor defect)	 $\varphi = (a + b)/2$ Distance between 2 defects should more than 3mm apart.
02	Electrical Defect (Minor defect)	(see table below) Remark: 1. Bright dot caused by scratch and foreign object accords to item 1.

Item 01 criteria table:

Size \ Area	Acc. Qty
$\varphi \leq 0.10$	Ignore
$0.10 < \varphi \leq 0.15$	2
$0.15 < \varphi \leq 0.25$	1
$0.25 < \varphi$	0
Total	2 no include $\varphi \leq 0.10$

Item 02 criteria table:

	Display Area	Total	
Bright dot	0	0	Note1
Dark dot	N≤2	N≤2	Note1
Total dot	N≤2	N≤2	Note1
Mura	Not visible through 5% ND filters.		Note2

03	Black and White line Scratch Foreign material (Line type) (Minor defect)	

Length	Width	Acc. Qty
/	$W \leqq 0.03$	Ignore
$L \leqq 2.5$	$0.03 < W \leqq 0.05$	3
$L \leqq 2.5$	$0.05 < W \leqq 0.10$	2
/	$0.1 < W$	
Total		3

Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.

04	Glass Crack (Minor defect)	

Crack is potential to enlarge, any type is not allowed.

05	Glass Chipping Pad Area: (Minor defect)	

Length and Width	Acc. Qty
c > 3.0, b< 1.0	1
c< 3.0, b< 1.0	3
a<Glass Thickness	

06	Glass Chipping Rear of Pad Area: (Minor defect)	

Length and Width	Acc. Qty
c > 3.0, b< 1.0	1
c< 3.0, b< 1.0	2
c< 3.0, b< 0.5	4
a<Glass Thickness	

07	Glass　Chipping Except Pad Area: (Minor defect) 		

For item 07:

Length and Width	Acc. Qty
c > 3.0, b< 1.0	1
c< 3.0, b< 1.0	2
c< 3.0, b< 0.5	4
a<Glass Thickness	

08 Glass Corner Chipping:
(Minor defect)

Length and Width	Acc. Qty
c < 3.0, b< 3.0	Ignore
a<Glass Thickness	

09 Glass Burr:
(Minor defect)

Length	Acc. Qty
F < 1.0	Ignore

Glass burr don't affect assemble and module dimension.

10	FPC Defect: (Minor defect)	10.1 Dent, pinhole width a<w/3. (w: circuitry width.) 10.2 Open circuit is unacceptable. 10.3 No oxidation, contamination and distortion.

11	Bubble on Polarizer (Minor defect)	Diameter	Acc. Qty
		φ≤0.20	Ignore
		0.20 <φ≤0.30	4
		0.30 <φ≤0.50	1
		0.50 < φ	None

12	Dent on Polarizer (Minor defect)	Diameter	Acc. Qty
		φ≤0.20	Ignore
		0.20 <φ≤0.30	4
		0.30 <φ≤0.50	1
		0.50 < φ	None

13	Bezel	13.1 No rust, distortion on the Bezel. 13.2 No visible fingerprints, stains or other contamination.
14	PCB	14.1 No distortion or contamination on PCB terminals. 14.2 All components on PCB must same as documented on the BOM/component layout. 14.3 Follow IPC-A-600F.
15	Soldering	Follow IPC-A-610C standard
16	Electrical Defect (Major defect)	The below defects must be rejected. 16.1 Missing vertical / horizontal segment, 16.2 Abnormal Display. 16.3 No function or no display. 16.4 Current exceeds product specifications. 16.5 LCD viewing angle defect. 16.6 No Backlight. 16.7 Dark Backlight. 16.8 Touch Panel no function.

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

10.7.Classification of Defects

10.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

10.7.2. Two minor defects are equal to one major in lot sampling inspection.

10.8.Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

10.9.Packaging

10.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

10.9.2. Modules inside package box should have compliant mark.

10.9.3. All direct package materials shall offer ESD protection.

Note1: Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.
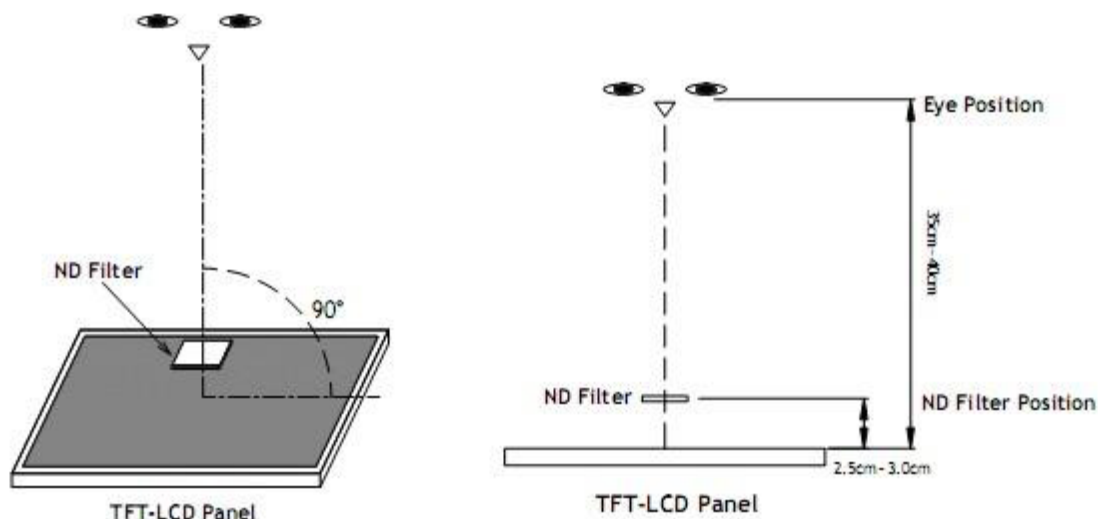
Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

11. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	**70℃, 96Hrs**	2	GB/T2423.2 -2008
2	Low Temperature Operating	**-20℃, 96Hrs**	2	GB/T2423.1 -2008
3	High Humidity Storage	**50℃, 90%RH, 96Hrs**	2	GB/T2423.3 -2016
4	High Temperature Storage	**80℃, 96Hrs**	2	GB/T2423.2 -2008
5	Low Temperature Storage	**-30℃, 96Hrs**	2	GB/T2423.1 -2008
6	Thermal Cycling Test Storage	-20℃, 60min~ 70℃, 60min, 20 cycles.	2	GB/T2423.22 -2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 30 min for each direction.	-	GB/T5170.14 -2009
8	Electrical Static Discharge	Air:±4KV 150pF/330Ω 5 times	2	GB/T17626.2 -2018
		Contact:±2KV 150pF/330Ω 5 times		
9	**Drop Test (Packaged)**	Height:80 cm,1 corner, 3 edges, 6 surfaces.	-	GB/T2423.7 -2018

Note1.　No defection cosmetic and operational function allowable.

Note2.　Total current Consumption should be below double of initial value

12. Precautions and Warranty

12.1. Safety

12.1.1.   The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

12.1.2.   Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

12.2. Handling

12.2.1.   Reverse and use within ratings in order to keep performance and prevent damage.

12.2.2.   Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

12.3. Storage

12.3.1.   Do not store the LCD module beyond the specified temperature ranges.

12.3.2.   Strong light exposure causes degradation of polarizer and color filter.

12.4. Metal Pin (Apply to Products with Metal Pins)

12.4.1.   Pins of LCD and Backlight

12.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

12.4.1.2. Recommended Soldering Conditions
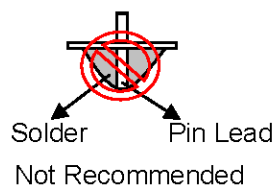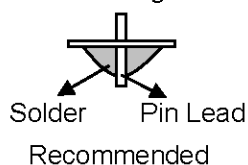
Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

12.4.1.3. Solder Wetting

Solder   Pin Lead   Solder   Pin Lead
Recommended   Not Recommended

12.4.2.   Pins of EL

12.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

12.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

12.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm
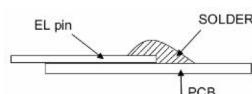
Recommended Solder Temperature: 270~290℃

Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

12.4.2.4. No horizontal press on the EL leads during soldering.

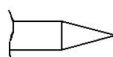12.4.2.5. 180° bend EL leads three times is not allowed.
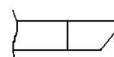
12.4.2.6. Solder Wetting

Recommended   Not Recommended
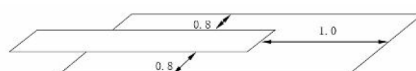
12.4.2.7. The type of the solder iron:

Recommended   Not Recommended

12.4.2.8. Solder Pad

12.5. Operation

12.5.1. Do not drive LCD with DC voltage

12.5.2. Response time will increase below lower temperature

12.5.3. Display may change color with different temperature

12.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear "fractured".

12.5.5. Do not connect or disconnect the LCM to or from the system when power is on.

12.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.

12.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

12.5.8. *Do not display the fixed pattern for long time（we suggest the time not longer than one hour）because it will develop image sticking due to the TFT structure.*

12.6. Static Electricity

12.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

12.6.2. The normal static prevention measures should be observed for work clothes and benches.

12.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

12.7. Limited Warranty

12.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

12.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

12.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

13. Packaging

TBD

Dimensions

- 75.33±0.2
- 73.93±0.2/LCD
- 0.80±0.2
- (1.79)
- 0.70±0.2
- (71.93)/A.A
- (1.70)
- 2.90±0.3

4.0" TFT
720(RGB)*720

- 79.52±0.2
- 78.02±0.2/LCD
- (71.93)/A.A
- Tear tape
- Single Area
- Components Area
- 48.45±0.5
- 22.81±0.5
- UL and E-number
- 3.00±0.3
- 30 ... 1
- W=0.30±0.05
- 0.50±0.1
- P0.5*39=14.50±0.05

- Contact side
- Stiffener
- 0.30±0.05
- SUS T=0.05
- 1 ... 30
- 5.00±0.3
- 15.50±0.1

K o ─[diodes]─ o A

Backlight LED Circuit:2×4=8(LED)
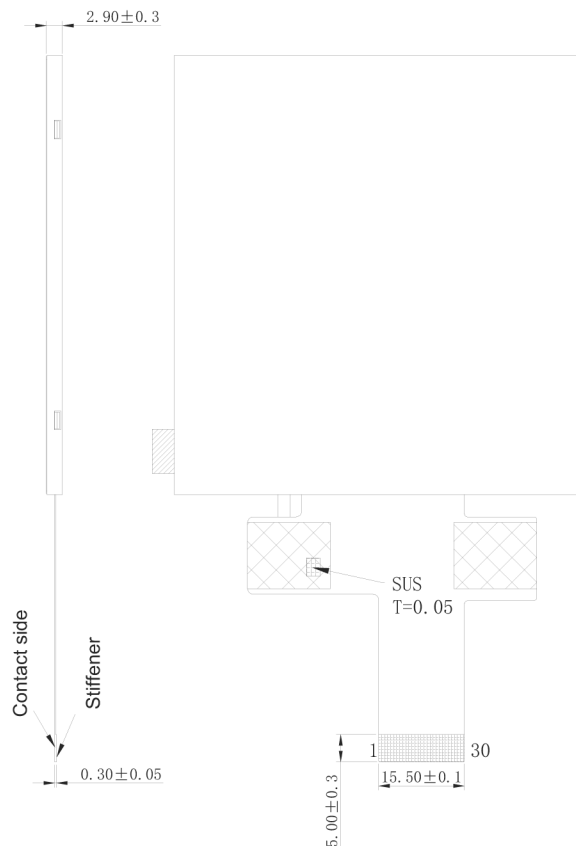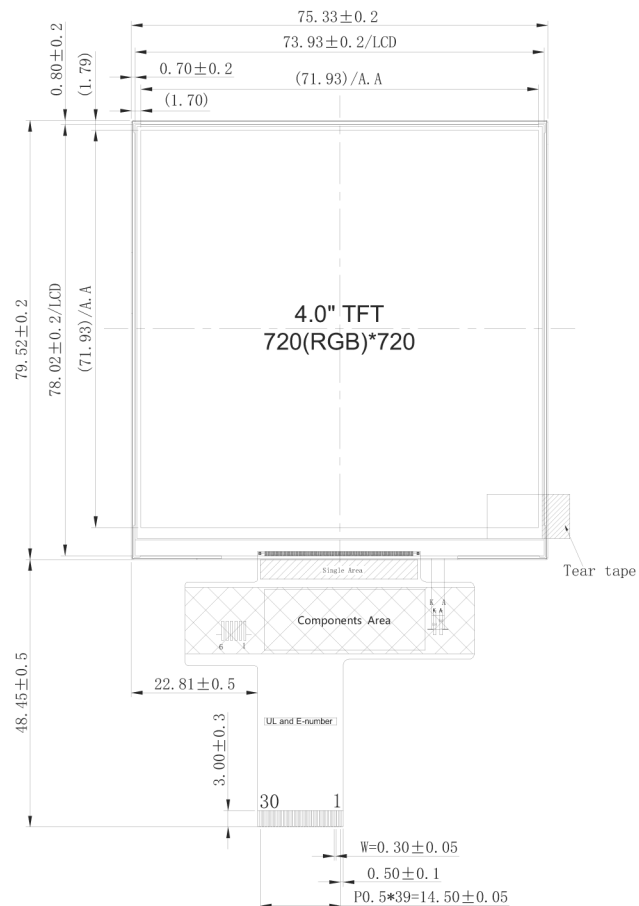
PIN FUNCTION

PIN	SYMBOL
1	LED K
2	LED A1
3	LED A2
4	VCI
5	IOVCC
6	RESET
7	TE
8	PWM
9	GND
10	D0_P
11	D0_N
12	GND
13	D1_P
14	D1_N
15	GND
16	CK_P
17	CK_N
18	GND
19	D2_P
20	D2_N
21	GND
22	D3_P
23	D3_N
24	GND
25	NC(TP_INT)
26	NC(TP_SDA)
27	NC(TP_SCL)
28	NC(TP_RST)
29	NC(TP_VCI)
30	NC(TP_IOVCC)

General Tolerance ±

DIM Level	1	2	3	4
0-5	0.05	0.1	0.1	0.2
5-10	0.05	0.1	0.1	0.2
10-50	0.05	0.1	0.2	0.3
50-100	0.1	0.2	0.3	0.5
100-150	0.1	0.2	0.5	0.8
Level Seclect				◎

Compliance: RohS III(2015/863/EU)

NOTES:
1. Display size:4.0"TFT IPS
2. Viewing direction:full view
3. Display mode:Transmissive/Normal Black
4. Operation temperature:-20°C ~ +70°C
5. Storage temperature:-30°C ~ +80°C
6. Driver IC:JD9365DA-H3
7. Power supply voltage:2.8V
8. Backlight :White(8LED)/12.8(TYP)V/40mA
9. LCM Luminance:370(TYP)cd/m²
10. Interface type:MIPI
11. RoHS must be complied
* The dimension with mark brackets "()" just for reference

Tolerances:			Date	Name			
			05/25	dr	**YDP LCD I S 400 MI**		
Modifications		Date	Name	knitter-switch	**30 57 92**	Page 26/26	