

PRODUCT SPECIFICATION

6.8” TFT LCD MODULE
MODEL: YDP LCD I 680 MI



- < ◇ > Preliminary Specification
- < ◆ > Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

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Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2023.01.10	LQ	Initial Release	

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1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	6.8"	
LCD type	IPS TFT	
Display Mode	Transmissive /Normally black	
Resolution	480 RGB x 1280	Pixels
View Direction	FULL VIEW	Best Image
Module Outline	66.12(H) x 171.79 (V) x 2.62 (T) (Note1)	mm
Active Area	60.22 (H) x 160.59 (V)	mm
Pixel Size	125.46 (H) x 125.46 (V)	um
Pixel Arrangement	RGB Stripe	
Display Colors	16.7M	
Interface	4 Lane MIPI	
With or without touch panel	Without	
Driver IC	ICNL9707	-
Operating Temperature	-20~75	°C
Storage Temperature	-30~85	°C
Weight	TBD	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

GND=0V, Ta=25°C

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V _{CI}	-0.3	6.6	V
	IOVCC	-0.3	3.3	V
Storage temperature	T _{STG}	-30	+85	°C
Operating temperature	T _{OP}	-20	+75	°C

Note 1: If Ta below 50°C, the maximal humidity is 90%RH, if Ta over 50°C, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10°C, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V _{CI}	3.0	3.3	3.6	V
	IOVCC	1.65	1.8	3.3	V
Logic High level input voltage	V _{IH}	0.7*IOVCC	-	IOVCC	mV
Logic Low level input voltage	V _{IL}	GND	-	0.3*IOVCC	mV
Logic High level Output voltage	V _{OH}	0.8*IOVCC	-	IOVCC	mV
Logic Low level Output voltage	V _{OL}	GND	-	0.2*IOVCC	mV
Current Consumption	Logic Analog	I _{CC+} I _{IN}	-	TBD	mA
All white					

5. Backlight Characteristic

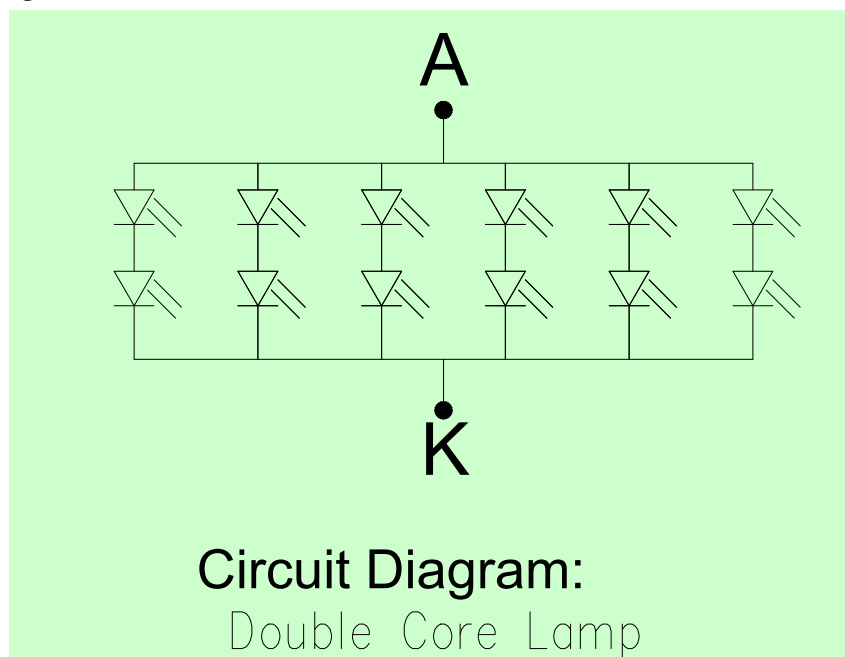
5.1. Backlight Characteristic

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V _F	T _a =25 °C, I _F =20mA/LED	11	12	13	V
Forward Current	I _F	T _a =25 °C, V _F =6V/LED	-	120	-	mA
Power dissipation	P _D		-	1440	-	mW
Uniformity	Avg		70	80	-	%
LED working life(25°C)	-		-	15,000	-	Hrs
Drive method	Constant current					
LED Configuration	12 White LEDs (2 LEDs in one string and 6 groups in parallel)					

Note1: LED life time defined as follows: The final brightness is at 50% of original brightness.

The environmental conducted under ambient air flow, at T_a=25±2 °C, 60%RH±5%, I_F=20mA/LED.

5.2. Backlight Characteristic



6. Optical Characteristics

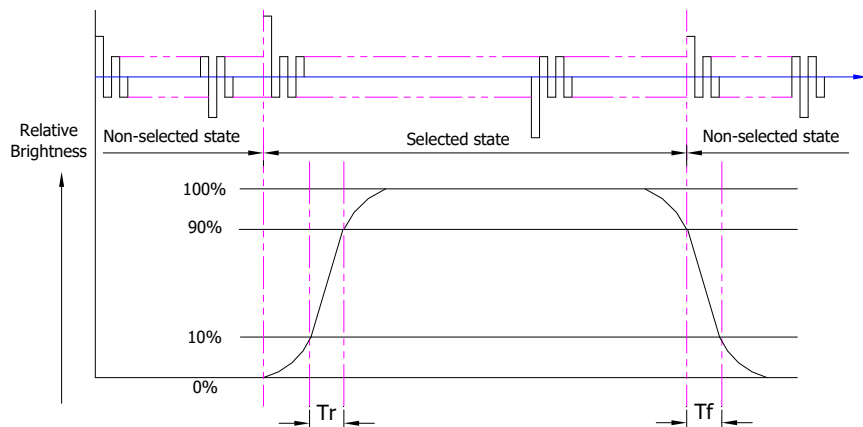
6.1. Optical Characteristics

Ta=25°C, VCI=3.3V

Backlight On (Transmissive Mode)	Item		Symbol	Condition	Specification			Unit
					Min.	Typ.	Max.	
	Luminance on TFT(I_f =20mA/LED)		Lv	Normally viewing angle $\theta_X = \varphi_Y = 0^\circ$	560	700	-	cd/m ²
	Contrast ratio(See 6.3)		CR		1000	1500	-	
	Response time (See 6.2)		T _R +T _F		-	25	35	ms
	Chromaticity Transmissive (See 6.5)	Red	X _R		-	TBD	-	
			Y _R		-	TBD	-	
		Green	X _G		-	TBD	-	
			Y _G		-	TBD	-	
		Blue	X _B		-	TBD	-	
			Y _B		-	TBD	-	
		White	X _W		-	TBD	-	
			Y _W		-	TBD	-	
	Viewing Angle (See 6.4)	Horizontal	θ _X +	Center CR≥10	70	80	-	Deg.
			θ _X -		70	80	-	
		Vertical	φ _Y +		70	80	-	
φ _Y -			70		80	-		
NTSC Ratio(Gamut)				65	70	-	%	

6.2. Definition of Response Time

6.2.1. Normally Black Type (Negative)

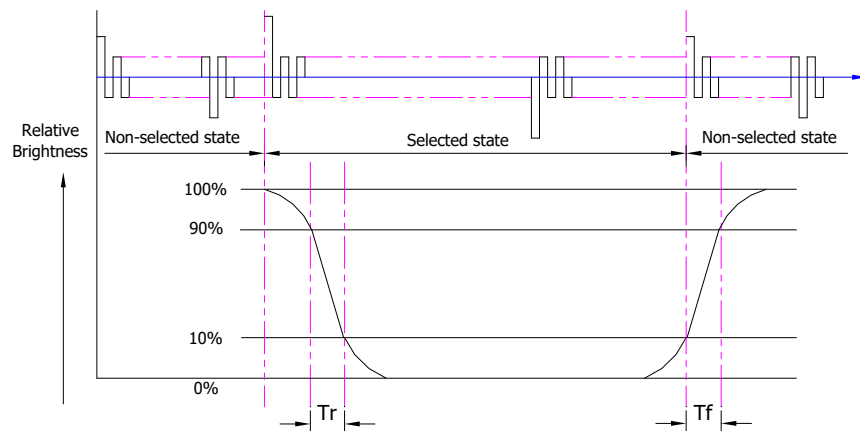


Tr is the time it takes to change from non-selected state with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note: Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)



Tr is the time it takes to change from non-selected state with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note: Measuring machine: LCD-5100 or EQUI

6.3. Definition of Contrast Ratio

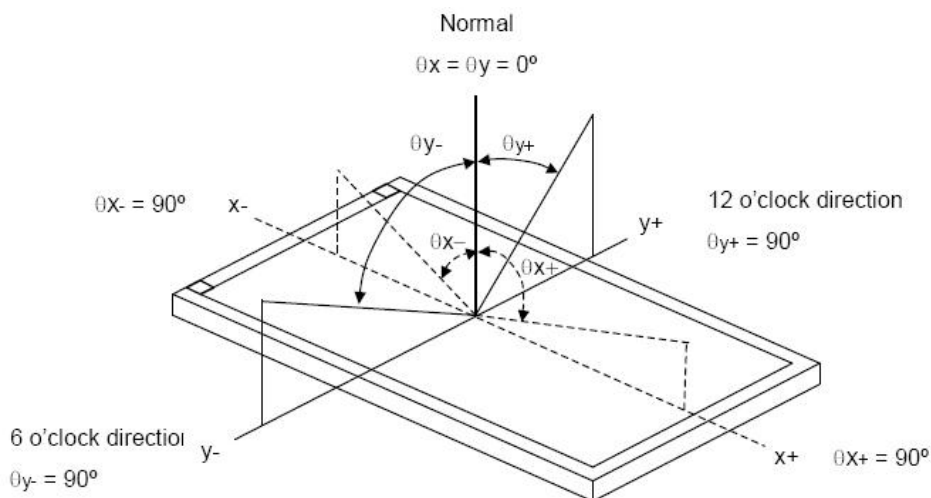
Contrast is measured perpendicular to display surface in reflective and transmissive mode.

The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

6.4. Definition of Viewing Angles



Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



6.6. Definition of Surface Luminance, Uniformity and Transmittance

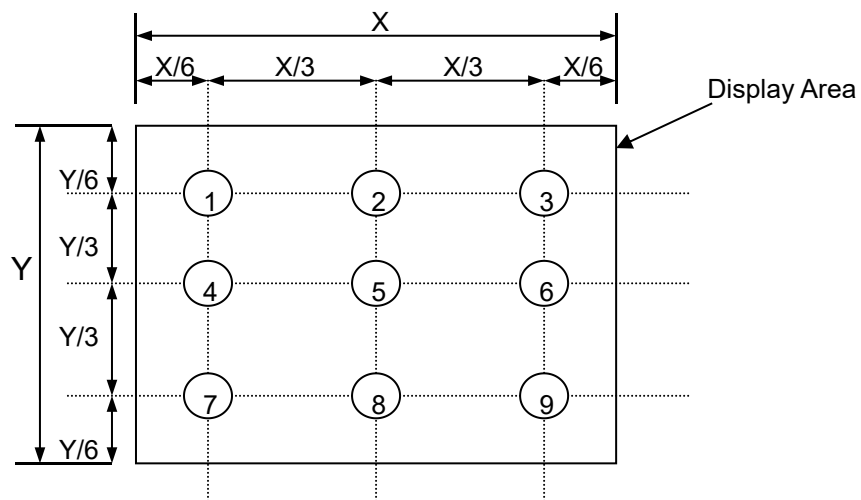
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1. Surface Luminance: $L_V = \text{average } (L_{P1}:L_{P9})$

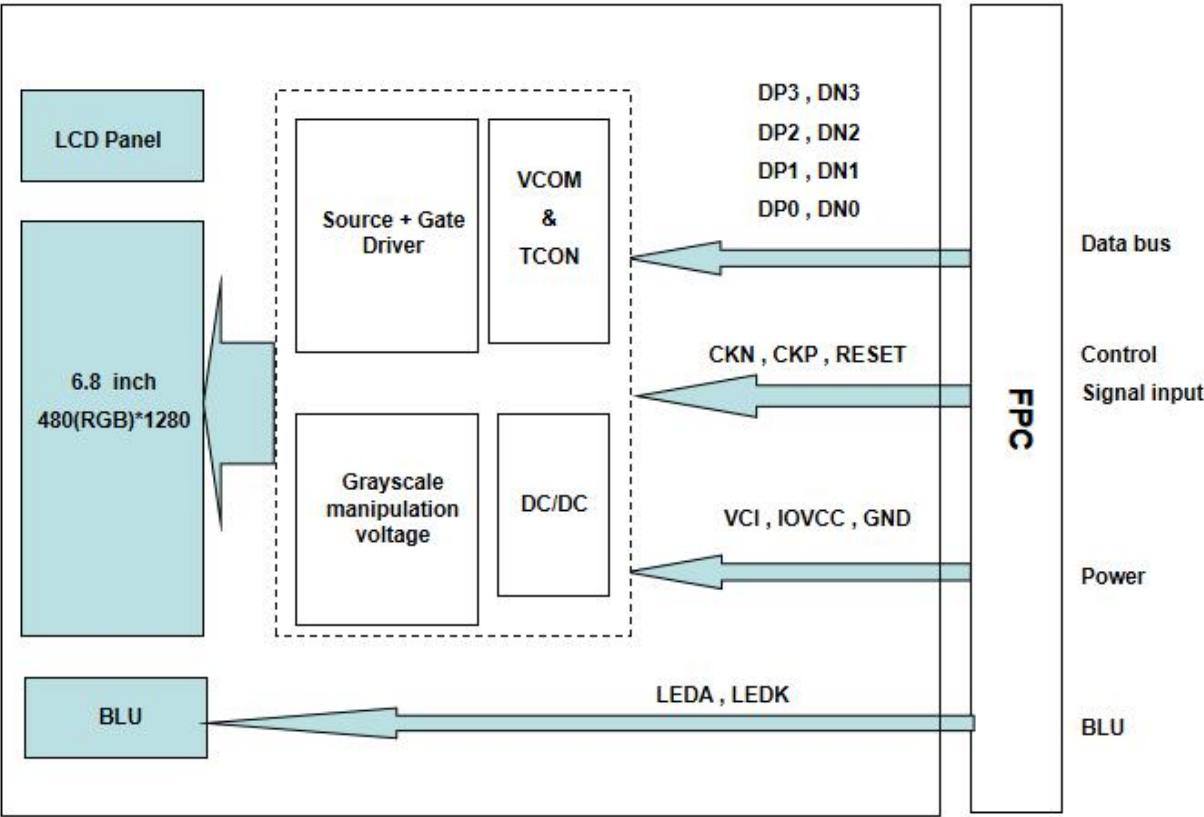
6.6.2. Uniformity = Minimal ($L_{P1}:L_{P9}$) / Maximal ($L_{P1}:L_{P9}$) * 100%

6.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note: Measuring machine: BM-7



7. Block Diagram and Power Supply



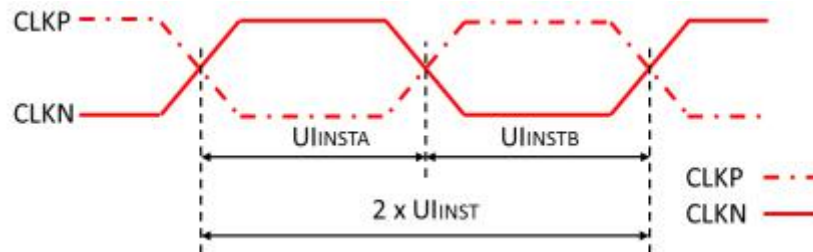
8. Interface Pins Definition

No.	Symbol	Function	Remark
1	GND	Ground	
2	VCI	A power supply for analog circuit	
3	VCI	A power supply for analog circuit	
4	IOVCC	A power supply for the logic power and I/O circuit	
5	GND	Ground	
6	RESET	Reset pin	
7	TE	No connection	
8	GND	Ground	
9	GND	Ground	
10	DN3	MIPI data Input	
11	DP3	MIPI data Input	
12	GND	Ground	
13	DN2	MIPI data Input	
14	DP2	MIPI data Input	
15	GND	Ground	
16	CKN	MIPI clock Input	
17	CKP	MIPI clock Input	
18	GND	Ground	
19	DN1	MIPI data Input	
20	DP1	MIPI data Input	
21	GND	Ground	
22	DN0	MIPI data Input	
23	DP0	MIPI data Input	
24	GND	Ground	
25	NC	No connection	
26	NC	No connection	
27	LEDK	Led cathode	
28	LEDK	Led cathode	
29	LEDA	Led anode	
30	LEDA	Led anode	

9. AC Characteristics

9.1. Timing Sequence

high speed mode – clock timing

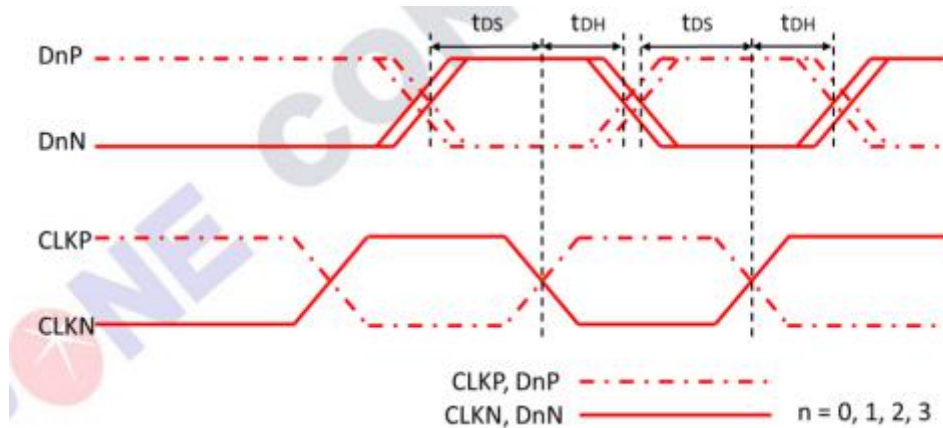


Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	$2 \times UI_{INST}$	Double UI instantaneous	2.5		12.5	ns	
CLK P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	1.25		6.25	ns	1,2

Note 1: $UI = UI_{INSTA} = UI_{INSTB}$.

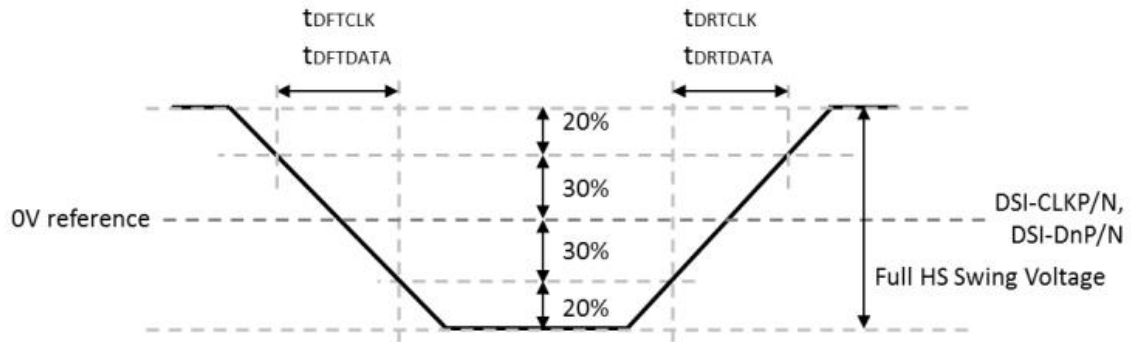
Note 2: ICNL9707 can support max 600Mbps/lane at 4 lane and max 800Mbps/lane at 3 lane application.

high speed mode – clock/data timing



Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	tDS	Data to Clock Setup time	$0.15 \times UI$			UI	
	tDH	Clock to Data Hold time	$0.15 \times UI$			UI	

high speed mode – rising and falling timing



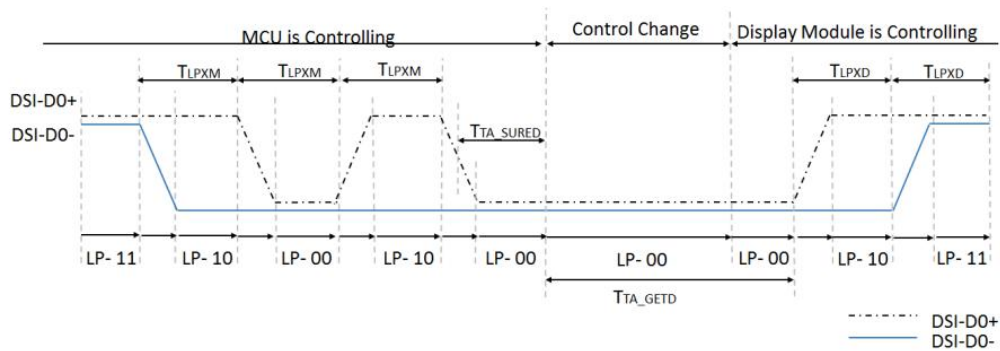
Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		$0.3 \cdot UI$		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		$0.3 \cdot UI$		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		$0.3 \cdot UI$		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		$0.3 \cdot UI$		1,2,3

Note 1: DnP/N, n =0,1,2 and 3.

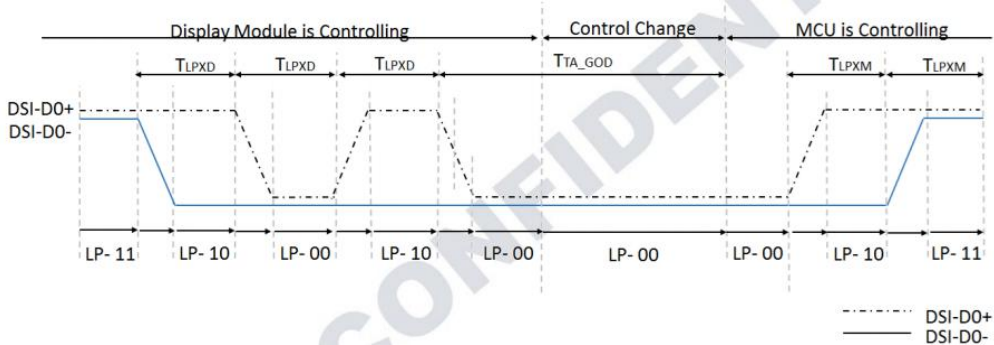
Note 2: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-PHY standard.

Note 3: DSI-CLK+ = CLKP, DSI-CLK- = CLKN, DSI-D0+ = D0P, DSI-D0- = D0N.

Low Speed Mode - Bus Turn Around



Bus Turnaround (BTA) from MCU to display module Timing

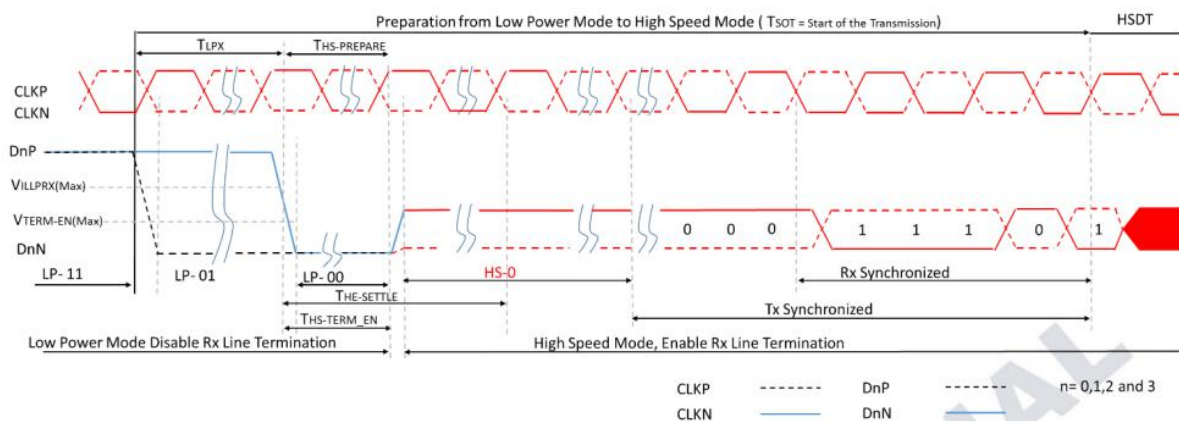


Bus Turnaround (BTA) from Display module to MCU Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		$2 * T_{LPXD}$	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	$5 * T_{LPXD}$			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request -MCU	$4 * T_{LPXD}$			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-.

Data Lanes from Low Power Mode to High Speed Mode

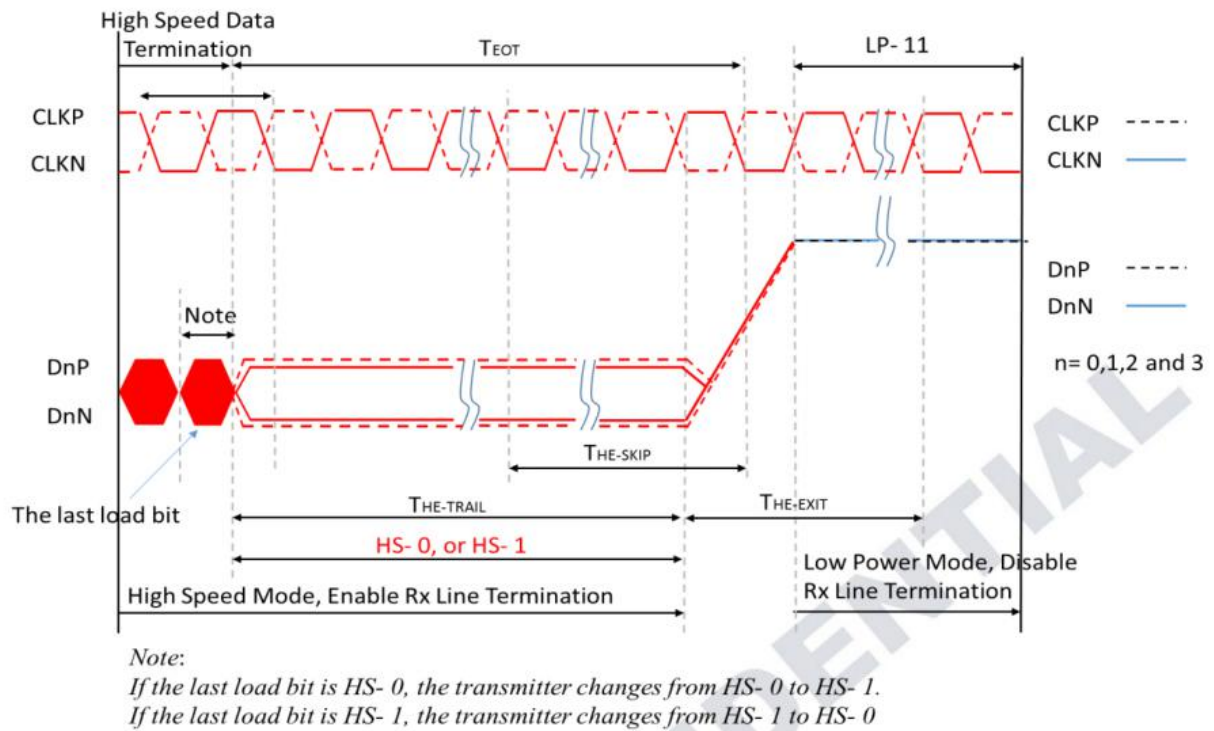


Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T_{LPX}	Length of any Low Power State Period	50			nS	1
DnP/N	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4*UI$		$85+6*UI$	nS	1
DnP/N	$T_{HS-TREM-EN}$	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			$35+4*UI$	nS	1

Note 1: DnP/N, $n=0,1,2 \text{ and } 3$.

Data Lanes from High Speed Mode to Low Power Mode

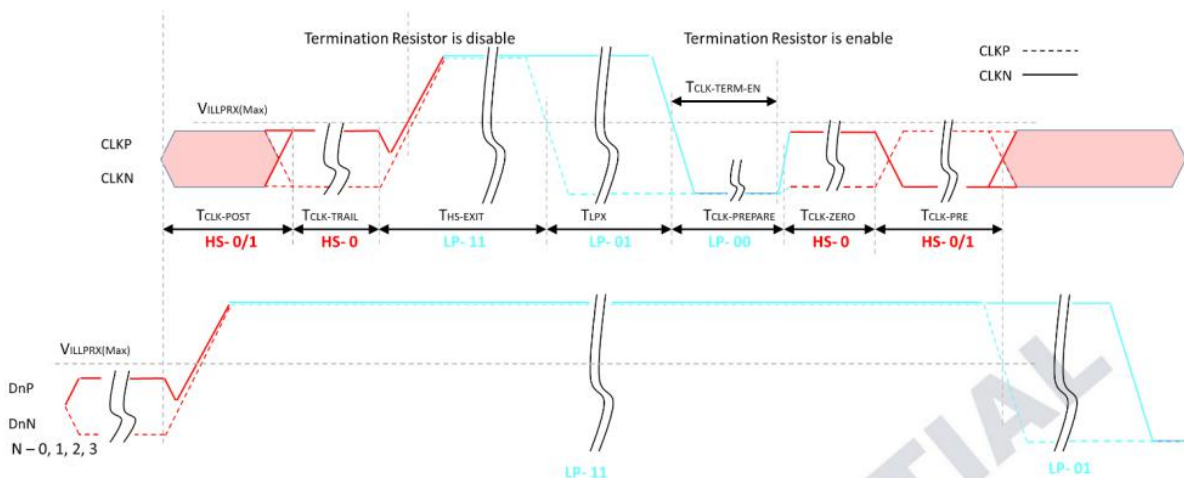


Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T _{HS-SKIP}	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=0, 1, 2 and 3.

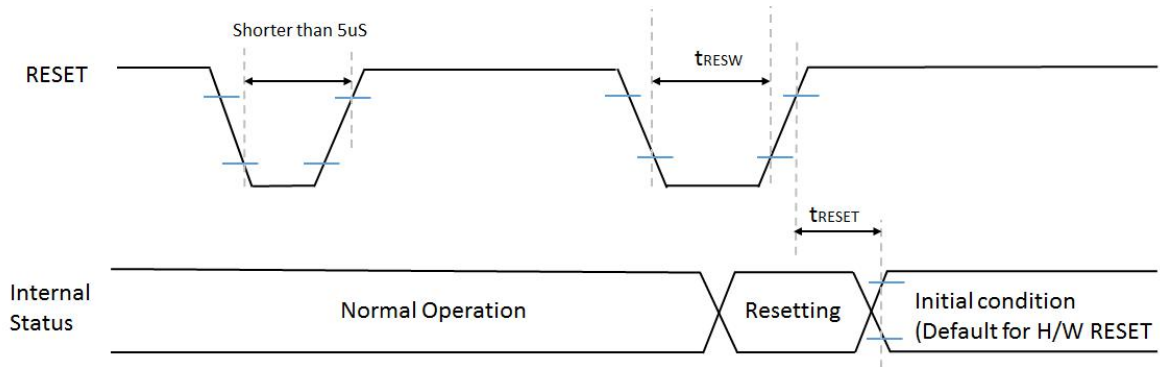
DSI Clock Burst – High speed mode to /from Low Power Mode



Clock Lane –High speed mode to / from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	T _{CK-POST}	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100			nS	
CKP/N	T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	T _{CLK-TERM-EN}	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	T _{CLK-PREPARE+} T _{CLK-ZERO}	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

9.2. Reset timing



Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	t_{RESW}	Reset "L" pulse width		10			uS	1
	t_{RESET}	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

Note 1: Condition : $T_a = 25^{\circ}\text{C}$.

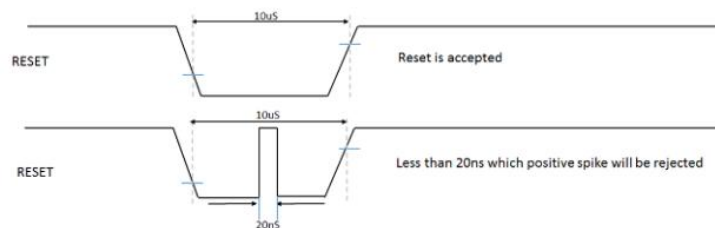
Note 2: Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Less than 5uS	Reset Rejected
More than 10uS	Reset
Between 5uS and 10uS	Reset Start

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (t_{RESET}) within 5ms after a rising edge of RESET.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: It is necessary to wait 5ms after releasing RESET when sending commands, and Sleep Out command can not be sent within 120ms.

10. Quality Assurance

10.1.Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

10.2.Standard for Quality Test

10.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

10.2.2. Sampling Criteria:

Visual inspection: AQL 1.5

Electrical functional: AQL 0.65.

10.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

10.3.Nonconforming Analysis & Disposition

10.3.1. Nonconforming analysis:

10.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

10.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

10.3.1.3. If cannot finish the analysis on time, customer will be notified with the progress status.

10.3.2. Disposition of nonconforming:

10.3.2.1. Non-conforming product over PPM level will be replaced.

10.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

10.4.Agreement Items

Shall negotiate with customer if the following situation occurs:

10.4.1. There is any discrepancy in standard of quality assurance.

10.4.2. Additional requirement to be added in product specification.

10.4.3. Any other special problem.

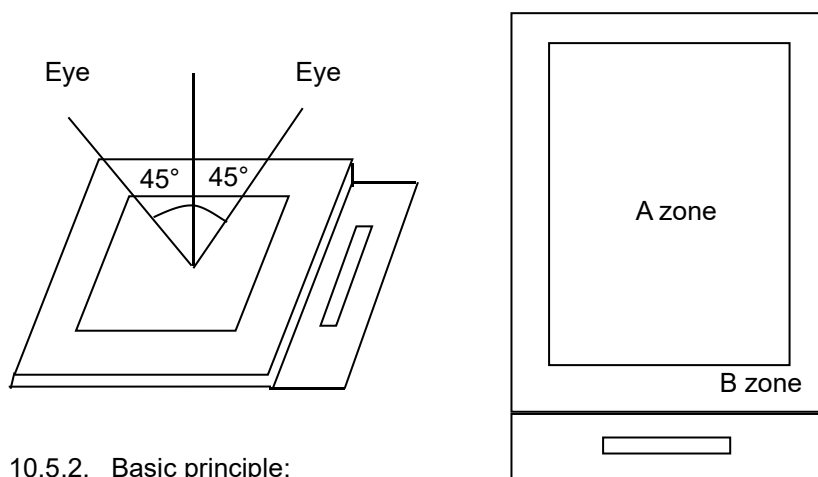
10.5.Standard of the Product Visual Inspection

10.5.1. Appearance inspection:

10.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

10.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

10.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,

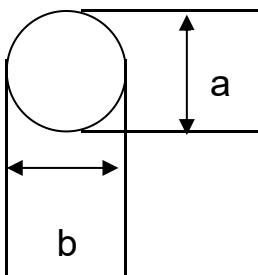


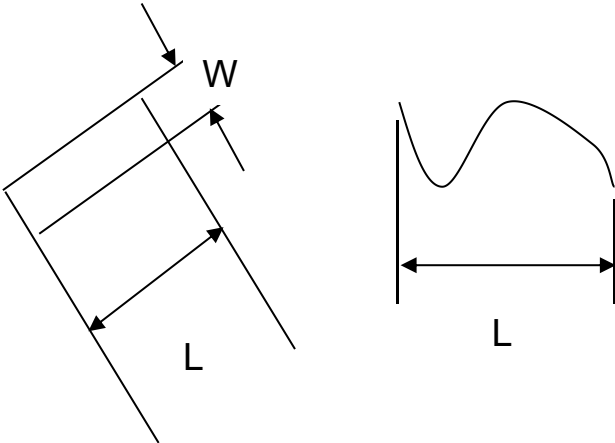
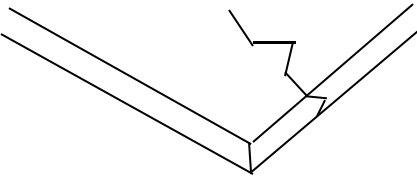
10.5.2. Basic principle:

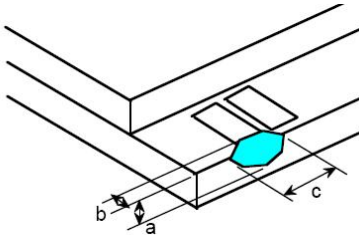
10.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

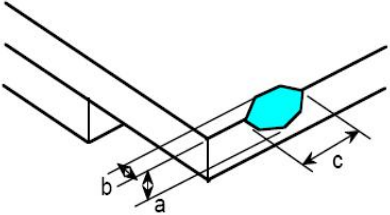
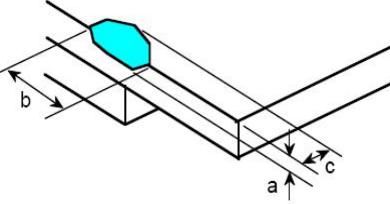
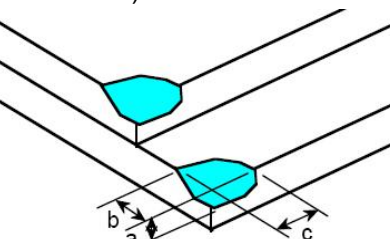
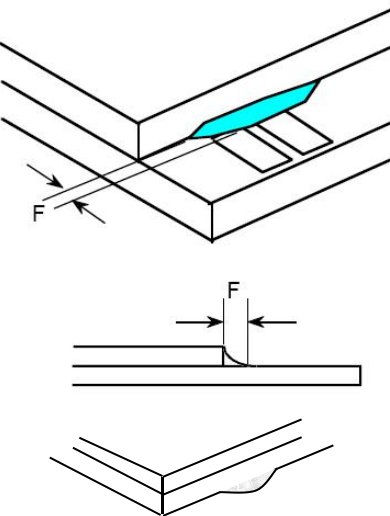
10.5.2.2. New item must be added on time when it is necessary.

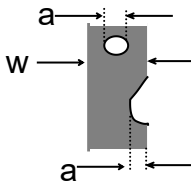
10.6. Inspection Specification

No.	Item	Criteria (Unit: mm)																			
01	Black / White spot Foreign material (Round type) Pinholes Stain Particles inside cell. (Minor defect)	 $\varphi = (a + b) / 2$ Distance between 2 defects should more than 3mm apart.	<table><tr><th>Size \ Area</th><th>Acc. Qty</th></tr><tr><td>$\varphi \leq 0.20$</td><td>Ignore</td></tr><tr><td>$0.20 < \varphi \leq 0.50$</td><td>$N \leq 3$</td></tr><tr><td>$0.50 < \varphi$</td><td>0</td></tr></table>	Size \ Area	Acc. Qty	$\varphi \leq 0.20$	Ignore	$0.20 < \varphi \leq 0.50$	$N \leq 3$	$0.50 < \varphi$	0										
Size \ Area	Acc. Qty																				
$\varphi \leq 0.20$	Ignore																				
$0.20 < \varphi \leq 0.50$	$N \leq 3$																				
$0.50 < \varphi$	0																				
02	Electrical Defect (Minor defect)	<table><tr><td></td><td>Display Area</td><td>Total</td><td rowspan="4">Note 1</td></tr><tr><td>Bright dot</td><td>$N \leq 2$</td><td>$N \leq 2$</td></tr><tr><td>Dark dot</td><td>$N \leq 4$</td><td>$N \leq 4$</td></tr><tr><td>Total dot</td><td>$N \leq 4$</td><td>$N \leq 4$</td></tr><tr><td>Mura</td><td colspan="2">Not visible through 5% ND filters.</td><td>Note 2</td></tr></table> Remark: 1. Bright dot caused by scratch and foreign object accords to item 1.				Display Area	Total	Note 1	Bright dot	$N \leq 2$	$N \leq 2$	Dark dot	$N \leq 4$	$N \leq 4$	Total dot	$N \leq 4$	$N \leq 4$	Mura	Not visible through 5% ND filters.		Note 2
	Display Area	Total	Note 1																		
Bright dot	$N \leq 2$	$N \leq 2$																			
Dark dot	$N \leq 4$	$N \leq 4$																			
Total dot	$N \leq 4$	$N \leq 4$																			
Mura	Not visible through 5% ND filters.		Note 2																		

03	Black and White line Scratch Foreign material (Line type) (Minor defect)	 <table border="1" data-bbox="612 748 1238 1055"> <thead> <tr> <th>Length</th><th>Width</th><th>Acc. Qty</th></tr> </thead> <tbody> <tr> <td>/</td><td>$W \leq 0.03$</td><td>Ignore</td></tr> <tr> <td>$L \leq 2.5$</td><td>$0.03 < W \leq 0.05$</td><td>3</td></tr> <tr> <td>$L \leq 2.5$</td><td>$0.05 < W \leq 0.10$</td><td>2</td></tr> <tr> <td>/</td><td>$0.1 < W$</td><td>0</td></tr> <tr> <td colspan="2">Total</td><td>3</td></tr> </tbody> </table> Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.	Length	Width	Acc. Qty	/	$W \leq 0.03$	Ignore	$L \leq 2.5$	$0.03 < W \leq 0.05$	3	$L \leq 2.5$	$0.05 < W \leq 0.10$	2	/	$0.1 < W$	0	Total		3
Length	Width	Acc. Qty																		
/	$W \leq 0.03$	Ignore																		
$L \leq 2.5$	$0.03 < W \leq 0.05$	3																		
$L \leq 2.5$	$0.05 < W \leq 0.10$	2																		
/	$0.1 < W$	0																		
Total		3																		
04	Glass Crack (Minor defect)	 Crack is potential to enlarge, any type is not allowed.																		

05	Glass Chipping Pad Area: (Minor defect)		<table><tr><th>Length and Width</th><th>Acc. Qty</th></tr><tr><td>$c > 3.0, b < 1.0$</td><td>1</td></tr><tr><td>$c < 3.0, b < 1.0$</td><td>3</td></tr><tr><td colspan="2">$a < \text{Glass Thickness}$</td></tr></table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	3	$a < \text{Glass Thickness}$	
	Length and Width	Acc. Qty									
$c > 3.0, b < 1.0$	1										
$c < 3.0, b < 1.0$	3										
$a < \text{Glass Thickness}$											

06	Glass Chipping Rear of Pad Area: (Minor defect) 	<table><tr><th>Length and Width</th><th>Acc. Qty</th></tr><tr><td>$c > 3.0, b < 1.0$</td><td>1</td></tr><tr><td>$c < 3.0, b < 1.0$</td><td>2</td></tr><tr><td>$c < 3.0, b < 0.5$</td><td>4</td></tr><tr><td colspan="2">$a < \text{Glass Thickness}$</td></tr></table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	2	$c < 3.0, b < 0.5$	4	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	2											
$c < 3.0, b < 0.5$	4											
$a < \text{Glass Thickness}$												
07	Glass Chipping Except Pad Area: (Minor defect) 	<table><tr><th>Length and Width</th><th>Acc. Qty</th></tr><tr><td>$c > 3.0, b < 1.0$</td><td>1</td></tr><tr><td>$c < 3.0, b < 1.0$</td><td>2</td></tr><tr><td>$c < 3.0, b < 0.5$</td><td>4</td></tr><tr><td colspan="2">$a < \text{Glass Thickness}$</td></tr></table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	2	$c < 3.0, b < 0.5$	4	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	2											
$c < 3.0, b < 0.5$	4											
$a < \text{Glass Thickness}$												
08	Glass Corner Chipping: (Minor defect) 	<table><tr><th>Length and Width</th><th>Acc. Qty</th></tr><tr><td>$c < 3.0, b < 3.0$</td><td>Ignore</td></tr><tr><td colspan="2">$a < \text{Glass Thickness}$</td></tr></table>	Length and Width	Acc. Qty	$c < 3.0, b < 3.0$	Ignore	$a < \text{Glass Thickness}$					
Length and Width	Acc. Qty											
$c < 3.0, b < 3.0$	Ignore											
$a < \text{Glass Thickness}$												
09	Glass Burr: (Minor defect) 	<table><tr><th>Length</th><th>Acc. Qty</th></tr><tr><td>$F < 1.0$</td><td>Ignore</td></tr></table> Glass burr don't affect assemble and module dimension.	Length	Acc. Qty	$F < 1.0$	Ignore						
Length	Acc. Qty											
$F < 1.0$	Ignore											

10	FPC Defect: (Minor defect) 	10.1 Dent, pinhole width $a < w/3$. (w: circuitry width.) 10.2 Open circuit is unacceptable. 10.3 No oxidation, contamination and distortion.										
11	Bubble on Polarizer (Minor defect)	<table><tr><th>Diameter</th><th>Acc. Qty</th></tr><tr><td>$\varphi \leq 0.20$</td><td>Ignore</td></tr><tr><td>$0.20 < \varphi \leq 0.30$</td><td>4</td></tr><tr><td>$0.30 < \varphi \leq 0.50$</td><td>1</td></tr><tr><td>$0.50 < \varphi$</td><td>None</td></tr></table>	Diameter	Acc. Qty	$\varphi \leq 0.20$	Ignore	$0.20 < \varphi \leq 0.30$	4	$0.30 < \varphi \leq 0.50$	1	$0.50 < \varphi$	None
Diameter	Acc. Qty											
$\varphi \leq 0.20$	Ignore											
$0.20 < \varphi \leq 0.30$	4											
$0.30 < \varphi \leq 0.50$	1											
$0.50 < \varphi$	None											
12	Dent on Polarizer (Minor defect)	<table><tr><th>Diameter</th><th>Acc. Qty</th></tr><tr><td>$\varphi \leq 0.20$</td><td>Ignore</td></tr><tr><td>$0.20 < \varphi \leq 0.30$</td><td>4</td></tr><tr><td>$0.30 < \varphi \leq 0.50$</td><td>1</td></tr><tr><td>$0.50 < \varphi$</td><td>None</td></tr></table>	Diameter	Acc. Qty	$\varphi \leq 0.20$	Ignore	$0.20 < \varphi \leq 0.30$	4	$0.30 < \varphi \leq 0.50$	1	$0.50 < \varphi$	None
Diameter	Acc. Qty											
$\varphi \leq 0.20$	Ignore											
$0.20 < \varphi \leq 0.30$	4											
$0.30 < \varphi \leq 0.50$	1											
$0.50 < \varphi$	None											
13	Bezel	13.1 No rust, distortion on the Bezel. 13.2 No visible fingerprints, stains or other contamination.										
14	PCB	14.1 No distortion or contamination on PCB terminals. 14.2 All components on PCB must same as documented on the BOM/component layout. 14.3 Follow IPC-A-600F.										
15	Soldering	Follow IPC-A-610C standard										
16	Electrical Defect (Major defect)	The below defects must be rejected. 16.1 Missing vertical / horizontal segment, 16.2 Abnormal Display. 16.3 No function or no display. 16.4 Current exceeds product specifications. 16.5 LCD viewing angle defect. 16.6 No Backlight. 16.7 Dark Backlight. 16.8 Touch Panel no function.										

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

10.7. Classification of Defects

10.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

10.7.2. Two minor defects are equal to one major in lot sampling inspection.

10.8. Identification/marketing criteria

Any unit with illegible / wrong / double or no marking/ label shall be rejected.

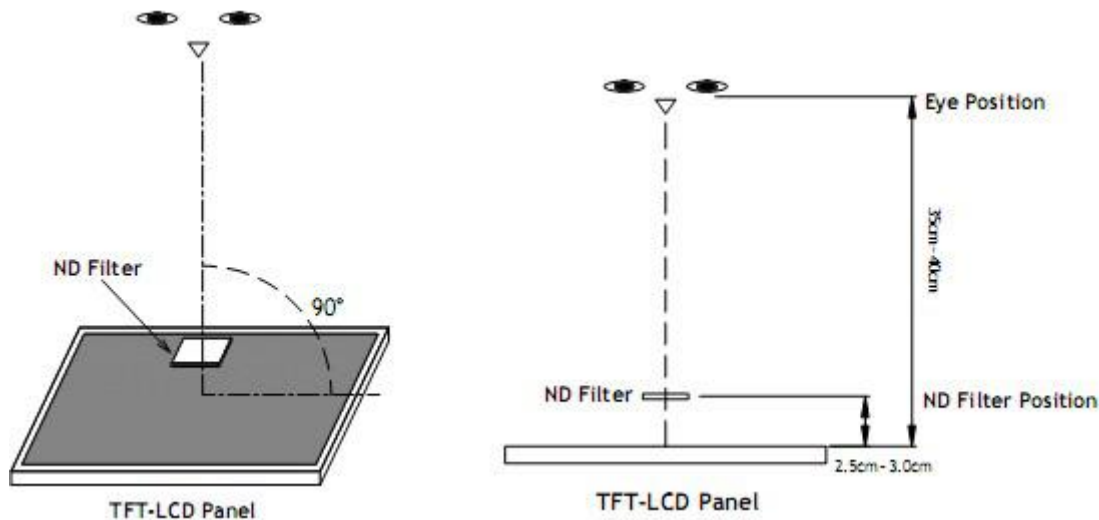
10.9. Packing

10.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

10.9.2. Modules inside package box should have compliant mark.

10.9.3. All direct package materials shall offer ESD protection.

Note1: Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.



Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is $350\text{mm} \pm 50\text{mm}$.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is $350\text{mm} \pm 50\text{mm}$.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

11. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	75°C, 96Hrs	2	GB/T2423.2-2008
2	Low Temperature Operating	-20°C, 96Hrs	2	GB/T2423.1-2008
3	High Humidity Storage	50°C, 90%RH, 96Hrs	2	GB/T2423.3-2016
4	High Temperature Storage	85°C, 96Hrs	2	GB/T2423.2-2008
5	Low Temperature Storage	-30°C, 96Hrs	2	GB/T2423.1-2008
6	Thermal Cycling Test Storage	-20°C, 60min ~ 75°C, 60min, 20 cycles.	2	GB/T2423.22-2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 30 min for each direction.	-	GB/T5170.14-2009
8	Electrical Static Discharge	Air: $\pm 4\text{KV}$ 150pF/330 Ω 5 times Contact: $\pm 2\text{KV}$ 150pF/330 Ω 5 times	2	GB/T17626.2-2018
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	-	GB/T2423.8-1995

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

12. Precautions and Warranty

12.1.Safety

- 12.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.
- 12.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

12.2.Handling

- 12.2.1. Reverse and use within ratings in order to keep performance and prevent damage.
- 12.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

12.3.Storage

- 12.3.1. Do not store the LCD module beyond the specified temperature ranges.
- 12.3.2. Strong light exposure causes degradation of polarizer and color filter.

12.4.Metal Pin (Apply to Products with Metal Pins)

12.4.1. Pins of LCD and Backlight

- 12.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

12.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

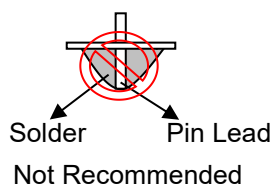
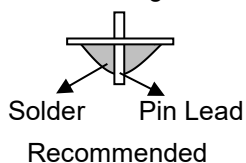
Maximum Solder Temperature: 370°C

Maximum Solder Time: 3s at the maximum temperature

Recommended Soldering Temp: 350±20°C

Typical Soldering Time: ≤3s

12.4.1.3. Solder Wetting



12.4.2. Pins of EL

- 12.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

- 12.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

12.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270~290°C

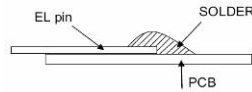
Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

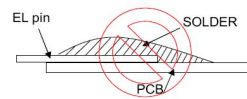
- 12.4.2.4. No horizontal press on the EL leads during soldering.

- 12.4.2.5. 180° bend EL leads three times is not allowed.
-

12.4.2.6. Solder Wetting

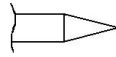


Recommended

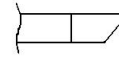


Not Recommended

12.4.2.7. The type of the solder iron:

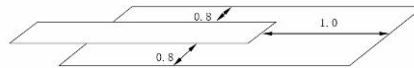


Recommended



Not Recommended

12.4.2.8. Solder Pad



12.5. Operation

- 12.5.1. Do not drive LCD with DC voltage
- 12.5.2. Response time will increase below lower temperature
- 12.5.3. Display may change color with different temperature
- 12.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.
- 12.5.5. Do not connect or disconnect the LCM to or from the system when power is on.
- 12.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.
- 12.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- 12.5.8. *Do not display the fixed pattern for long time (we suggest the time not longer than one hour) because it will develop image sticking due to the TFT structure.*

12.6. Static Electricity

- 12.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.
- 12.6.2. The normal static prevention measures should be observed for work clothes and benches.
- 12.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

12.7. Limited Warranty

- 12.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.
- 12.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.
- 12.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

13. Packaging

TBD

6.8" TFT-IPS 480RGB*1280

TEAR TAPE

66.12±0.25
60.22/A/A

(2.95)

160.59/A/A

171.79±0.3

27.7±0.3

5.15±0.5

81.12±0.3

15.5±0.1

5±0.5

Silk line

Component area

1 30

-25±0.2

0.3±0.05

Contact side

Silfener

66.12

2.62±0.2

(5)

Silk Line

0.5±0.1

P0.5*29=14.5

3±0.3

1 30

25.2±0.5

0.5max

Silk Line 20.15±0.5

1 30

Viewing after FPC bending
shipment with FPC Bending

PIN FUNCTION

PIN	SYMBOL	PIN FUNCTION
1	GND	
2	VCI	
3	VCI	
4	IOVCC	
5	GND	
6	RESET	
7	TE	
8	GND	
9	GND	
10	DN3	
11	DP3	
12	GND	
13	DN2	
14	DP2	
15	GND	
16	CKN	
17	CKP	
18	GND	
19	DN1	
20	DP1	
21	GND	
22	DN0	
23	DP0	
24	GND	
25	NC	
26	NC	
27	LEDK	
28	LEDK	
29	LEDA	
30	LEDA	

NOTES:

- Display size: 6.8" TFT
- Viewing direction: FULL VIEW/IPS
- Display mode: Transmissive/Normal Black
- Operation temperature: -20°C~+75°C
- Storage temperature: -30°C~+85°C
- Driver IC: ICN19707
- Power supply voltage: 3.3V
- Backlight: White (12 LED)/12V(TYP)/120mA
Brightness: 700(TYP)cd/m2
- RoHS must be complied
- Unspecified tolerance are ±0.2mm
- * The dimension with mark brackets "()" just for reference

Circuit Diagram:
Double Core Lamp

A

K

APPROVED

CHECKED

DRAWN

NO.

1/1

UNIT

mm

SCALE

VERSION

A

DATE

2023.1.08

MODEL

NAME: YDP LCD I 680 MI

TITLE:

Outline

FILE NAME:

REVISION RECORD

REV	REVISION	RECORD	SIGN	DATE
1	First Issue		LJB	23.1.08