PRODUCT SPECIFICATION

6.2” TFT LCD MODULE
MODEL: YDP LCD I 620 RI

ROHS

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY
TFT S. G. H 20221011	———	———	TFT L. Q 20221011

knitter-switch

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2022.09.16	LQ	Initial Release	
1.1	2022.09.22	LQ	Modify Outline Drawing(C)	P27
1.2	2022.10.11	LQ	Add Weight Add Current Consumption Add CIE Value Modify Outline Drawing(D)	P4 P5 P6 P27

Table of Contents

1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	6.2”	
LCD type	IPS TFT	
Display Mode	Transmissive /Normally black	
Resolution	640 RGB x 240	Pixels
View Direction	FULL VIEW	Best Image
Module Outline	163.6(H) x 67.6 (V) x 2.87 (T) (Note1)	mm
Active Area	148.8 (H) x 53.76 (V)	mm
Pixel Size	232.5 (H) x 224.0 (V)	um
Pixel Arrangement	RGB Vertical Stripe	
Polarizer Surface Treatment	Anti-Glare	
Display Colors	262K	
Interface	18-Bit RGB parallel + I^2C Interface	
With or without touch panel	Without	
Driver IC	ST5043AA+FL5894AA	-
Operating Temperature	**-20～70**	ºC
Storage Temperature	**-30～80**	ºC
Weight	60	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

GND=0V, Ta=25ºC

Item	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	-0.3	4.0	V
Storage temperature	T_{STG}	**-30**	**+80**	ºC
Operating temperature	T_{OP}	**-20**	**+70**	ºC

Note 1: If Ta below 50ºC, the maximal humidity is 90%RH, if Ta over 50ºC, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	3.0	3.3	3.6	V
Logic High level input voltage	V_{IH}	0.7*VDD	-	VDD	mV
Logic Low level input voltage	V_{IL}	0	-	0.3*VDD	mV
Logic High level Output voltage	V_{OH}	VDD-0.4	-	-	mV
Logic Low level Output voltage	V_{OL}	-	-	GND+0.4	mV
Current Consumption All white	I_{VDD}	-	75	-	mA

5. Backlight Characteristic

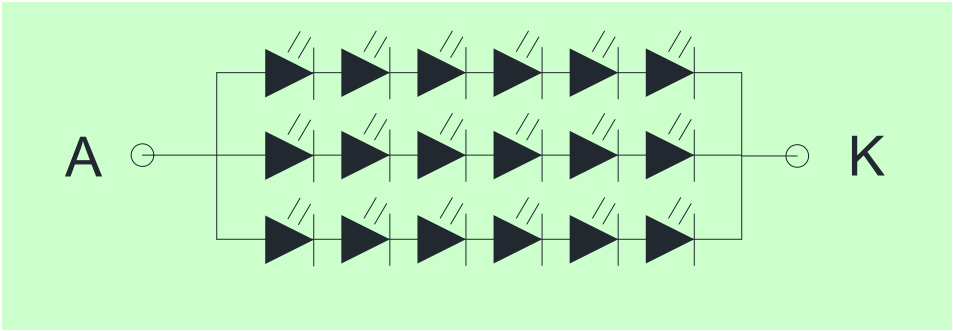
5.1. Backlight Characteristic

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V_F	Ta=25 ºC, I_F=20mA/LED	17.4	**19.2**	19.8	V
Forward Current	I_F	Ta=25 ºC, V_F=3.2V/LED	-	**60**	-	mA
Power dissipation	P_D		-	**1152**	-	mW
Uniformity	Avg		-	80	-	%
LED working life(25℃)	-		-	30,000	-	Hrs
Drive method	Constant current					
LED Configuration	18 White LEDs (6 LEDs in one string and 3 groups in parallel)					

Note1：LED life time defined as follows: The final brightness is at 50% of original brightness.

The environmental conducted under ambient air flow, at Ta=25±2 ºC,60%RH±5%, I_F=20mA/LED.

5.2. Backlight Characteristic



6. Optical Characteristics

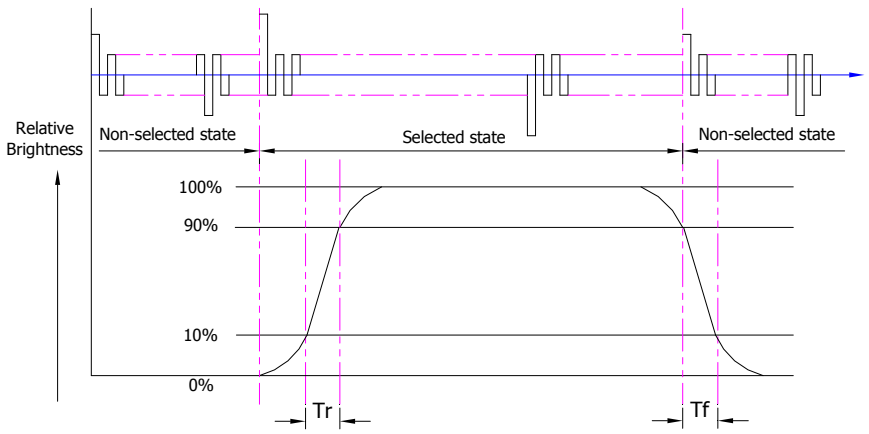
6.1. Optical Characteristics

Ta=25ºC, VDD=3.3V

	Item		Symbol	Condition	Specification			Unit
					Min.	Typ.	Max.	
Backlight On (Transmissive Mode)	Luminance on TFT(I_f =20mA/LED)		Lv	Normally viewing angle θX = φY =0º	**400**	**500**	-	cd/m²
	Contrast ratio(See 6.3)		CR		1000	1200	-	
	Response time (See 6.2)		TR+TF		-	25	35	ms
	Chromaticity Transmissive (See 6.5)	Red	XR		0.577	**0.627**	0.677	
			YR		0.309	**0.359**	0.409	
		Green	XG		0.271	**0.321**	0.371	
			YG		0.568	**0.618**	0.668	
		Blue	XB		0.084	**0.134**	0.184	
			YB		0.046	**0.096**	0.146	
		White	XW		0.234	**0.284**	0.334	
			YW		0.291	**0.341**	0.391	
	Viewing Angle (See 6.4)	Horizontal	θX+	Center CR≥10	80	85	-	Deg.
			θX-		80	85	-	
		Vertical	φY+		80	85	-	
			φY-		80	85	-	
	NTSC Ratio(Gamut)				65	70	-	%

6.2. Definition of Response Time

6.2.1. Normally Black Type (Negative)

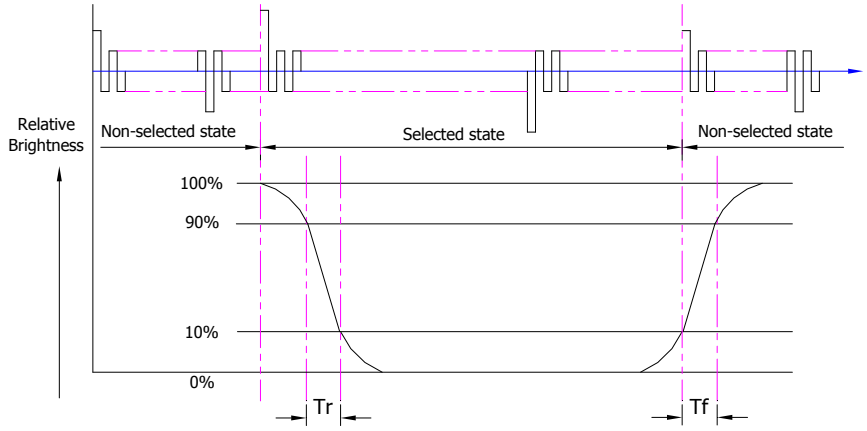


Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note: Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)



Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note: Measuring machine: LCD-5100 or EQUI

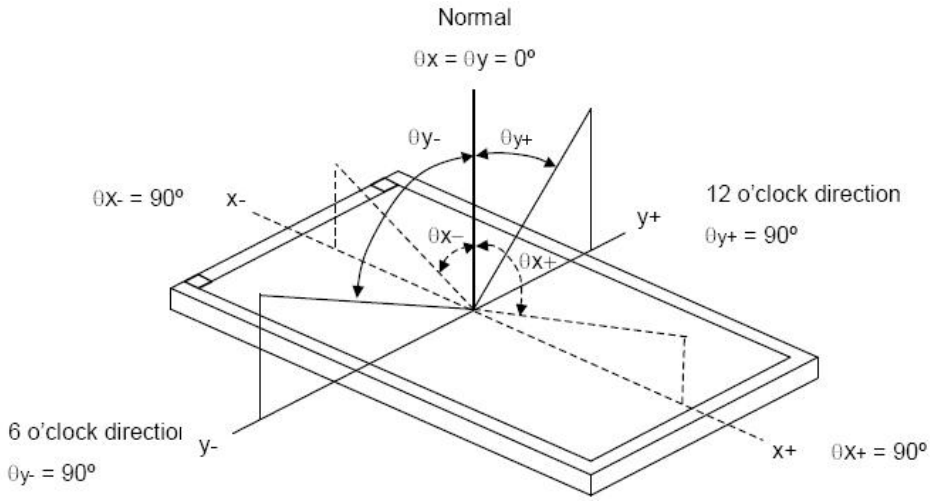
6.3. Definition of Contrast Ratio

Contrast is measured perpendicular to display surface in reflective and transmissive mode. The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

6.4. Definition of Viewing Angles



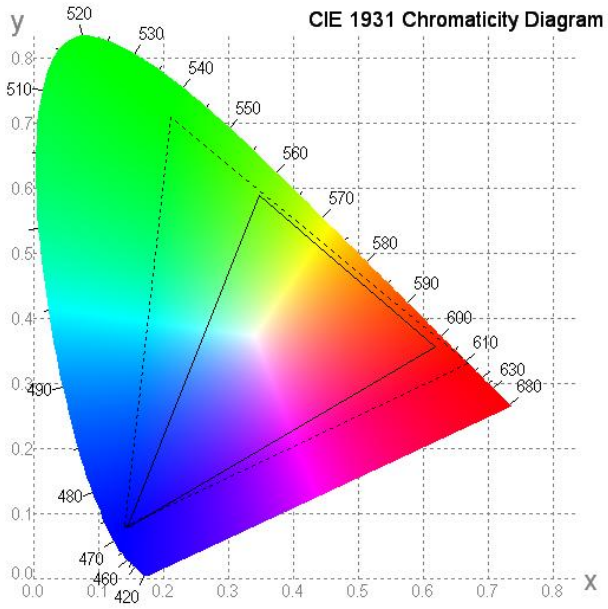
Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



6.6. Definition of Surface Luminance, Uniformity and Transmittance

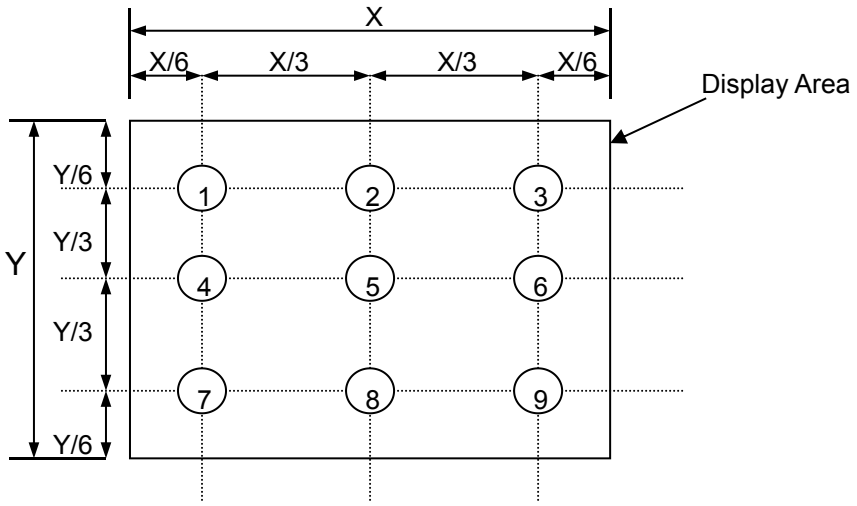
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1. Surface Luminance: L_V = average (L_{P1}:L_{P9})

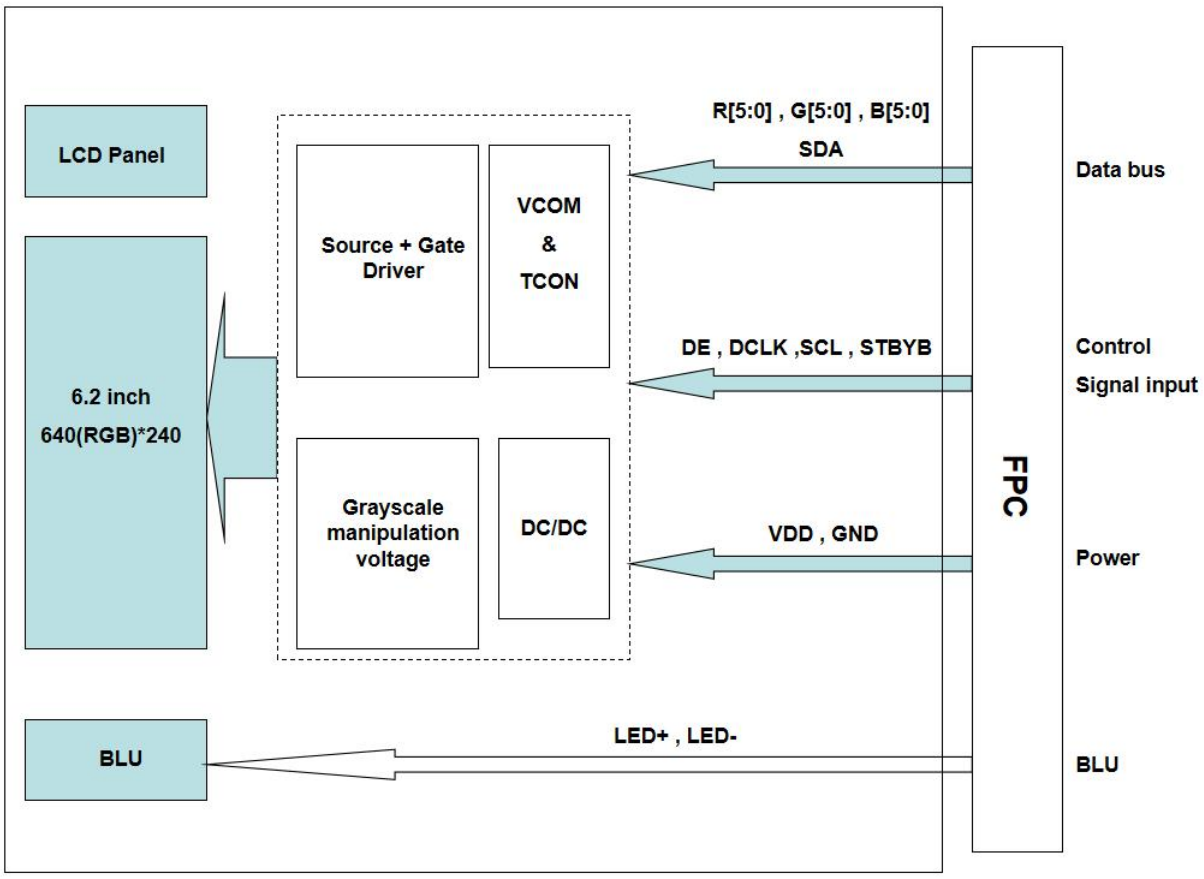
6.6.2. Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%

6.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note: Measuring machine: BM-7



7. Block Diagram and Power Supply



8. Interface Pins Definition

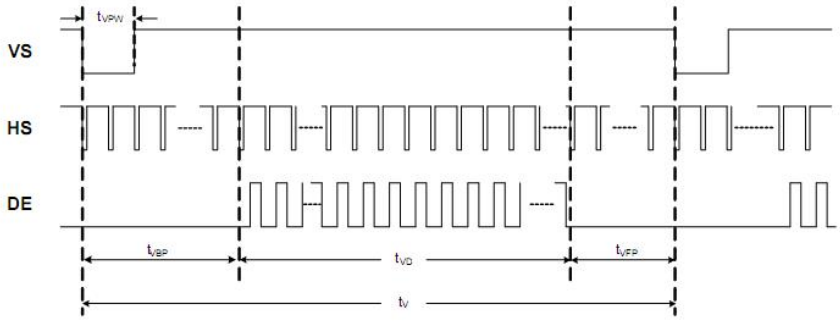
No.	Symbol	Function	Remark
1	VDD	A power supply for analog circuit	
2	VDD	A power supply for analog circuit	
3	VDD	A power supply for analog circuit	
4	VDD	A power supply for analog circuit	
5	VDD_MTP	No Connect	
6	DE	Data enable signal (DE) for DE mode	
7	GND	Ground	
8	DCLK	Clock input for TTL mode	
9	GND	Ground	
10	GND	Ground	
11	B5	Data input	
12	B4	Data input	
13	B3	Data input	
14	GND	Ground	
15	B2	Data input	
16	B1	Data input	
17	B0	Data input	
18	GND	Ground	
19	G5	Data input	
20	G4	Data input	
21	G3	Data input	
22	GND	Ground	
23	G2	Data input	
24	G1	Data input	
25	G0	Data input	
26	GND	Ground	
27	R5	Data input	
28	R4	Data input	
29	R3	Data input	
30	GND	Ground	
31	R2	Data input	
32	R1	Data input	
33	R0	Data input	
34	VCOM	VCOM OP buffer output. Connect a capacitor to stabilize output voltage.	
35	GND	Ground	
36	SDA	Serial address and data input/output for I2C interface.	
37	SCL	Clock signal for I2C interface.	
38	STBYB	H: Normal operation. (Default) ; L: Standby mode.	

39	LED+	Led cathode	
40	LED-	Led anode	

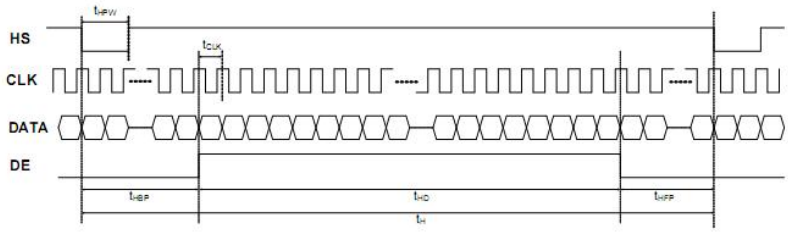
9. AC Characteristics

9.1. Input Timing

Vertical input timing



Horizontal input timing

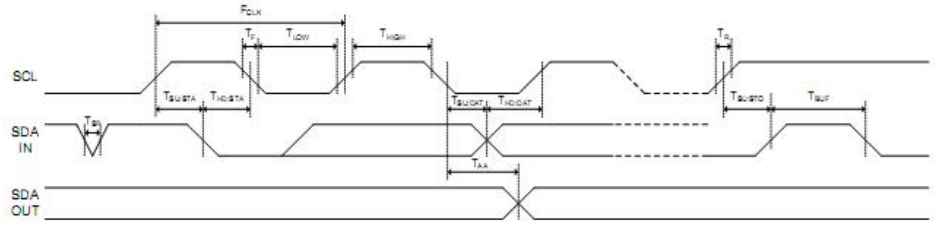


Timing Table

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
CLK frequency	t_{CLK}	20.0	24.2	31.2	Mhz
Horizontal display area	t_{HD}		640		t_{CLK}
Horizontal pulse width	t_{HPW}	2	2	255	t_{CLK}
Horizontal back porch	t_{HBP}	5	16	255	t_{CLK}
Horizontal front porch	t_{HFP}	24	120	260	t_{CLK}
Horizontal period	t_H	669	776	832	t_{CLK}
Vertical display area	t_{VD}		240		t_H
Vertical pulse width	t_{VPW}	1	8	20	t_H
Vertical back porch	t_{VBP}	2	12	255	t_H
Vertical front porch	t_{VFP}	5	22	260	t_H
Vertical period	t_V	487	282	624	t_H
Frame rate	FR	60	60	60	Hz

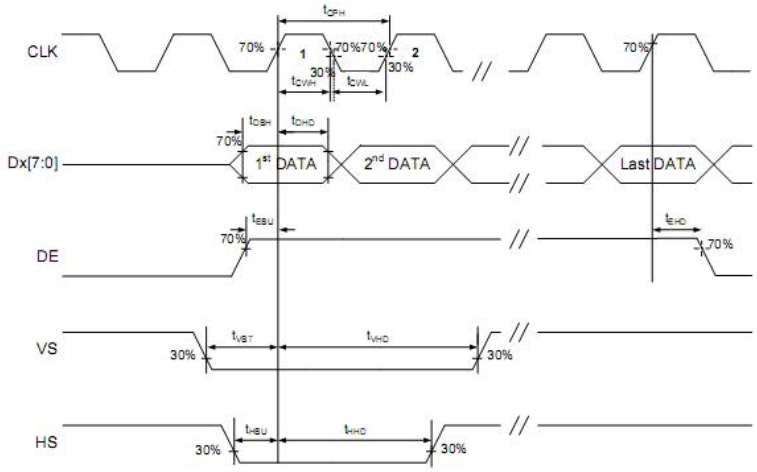
I2C Timing

Parameter	Signal	Symbol	Min	Typ.	Max.	Unit	Condition
Clock frequency	SCL	F_{CLK}	2500	-	-	ns	
Clock high time		T_{HIGH}	1250	-	-	ns	
Clock low time		T_{LOW}	1250	-	-	ns	
SDA and SCL rise time		T_R		-	300	ns	
SDA and SCL fall time		T_F		-	300	ns	
Start condition hold time	SDA IN	$T_{HD:STA}$	600	-	-	ns	
Start condition setup time		$T_{SU:STA}$	600	-	-	ns	
Data input hold time		$T_{HD:DAT}$	0	-	-	ns	
Data input setup time		$T_{SU:DAT}$	100	-	-	ns	
Stop condition setup time		$T_{SU:STO}$	600	-	-	ns	
Output valid from clock		T_{AA}	-	-	900	ns	
Input filter spike suppression (SDA and SCL pins)		T_{SP}	-	-	50	ns	
Bus free-time: Time the bus must be free before a new transmission can start	SDA OUT	T_{BUF}	1300	-	-	ns	



9.2. COMS AC CHARACTERISTICS

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
CLK cycle time	t_{CPH}	16.7			ns	
CLK pulse high duty	t_{CWH}	40	50	60	%	
CLK pulse low duty	t_{CWL}	40	50	60	%	
VS setup time	t_{VST}	4	-	-	ns	
VS hold time	t_{VHD}	2	-	-	ns	
HS setup time	t_{HST}	4	-	-	ns	
HS hold time	t_{HHD}	2	-	-	ns	
Data setup time	t_{DSH}	4	-	-	ns	D0[7:0], D1[7:0], D2[7:0], D3[7:0] to CLK
Date hold time	t_{DHD}	2	-	-	ns	D0[7:0], D1[7:0], D2[7:0], D3[7:0] to CLK
DE setup time	t_{ESU}	4	-	-	ns	
DE hold time	t_{EHD}	2	-	-	ns	



Note: This reference timing diagram set CK_POL=H, VS_POL=L and HS_POL=L

9.3. I2C interface

The I2C Compatible Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

Bit Transfer:

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in the figure below.

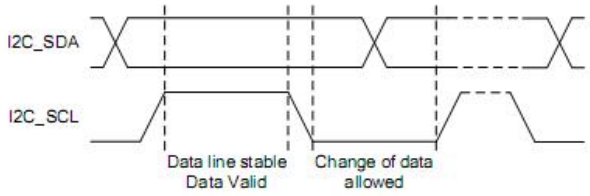


Fig. Bit Transfer

START and STOP Conditions:

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA while SCL is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in the figure below.

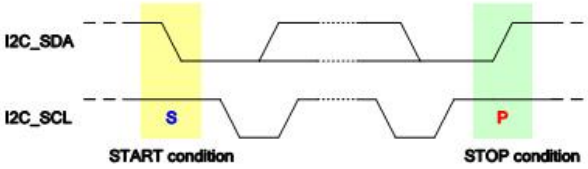


Fig. Definition of START and STOP Condition

Acknowledgement:

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter when the master generates an extra acknowledge-related clock pulse. A slave receiver addressed must generate an acknowledge-bit after the reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line stays LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the I2C Interface is illustrated in the figure below.

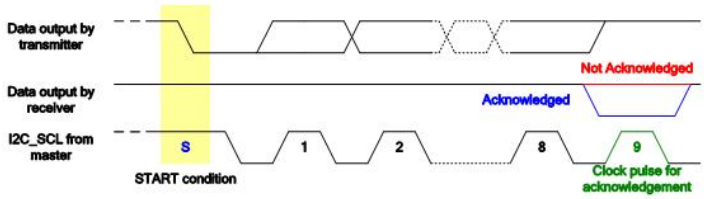
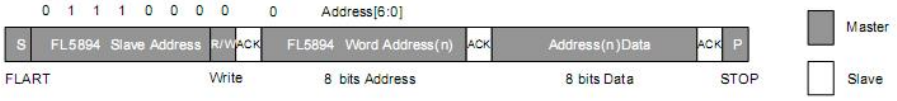


Fig. Acknowledgement of I2C Interface

I2C Interface Protocol:

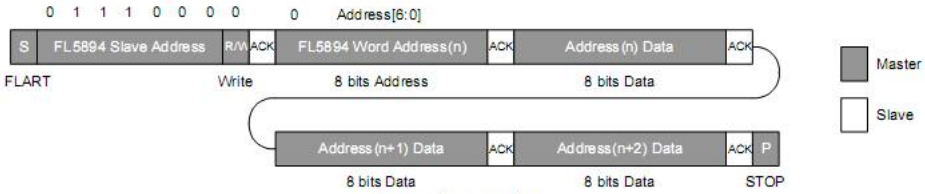
FL5894 supports 2-Wire Serial Interface (I2C) to set internal registers. The FL5894 acts as a slave device, and its slave address is fixed to 0111000.

The master device sends the START signal, the 7bit slave address "0111000," and the R/W=0 bit to inform the FL5894 that the master device is going to do the WRITE operation, and then the FL5894 will reply the first acknowledgement. After that, the master device sends 8-bit address to select which internal register to be set. The FL5894 will reply the second acknowledgement if the register address is valid. The master device sends 8-bit data for the internal register value, and then the FL5894 will reply the third acknowledgement. At last, the master device sends the STOP signal.



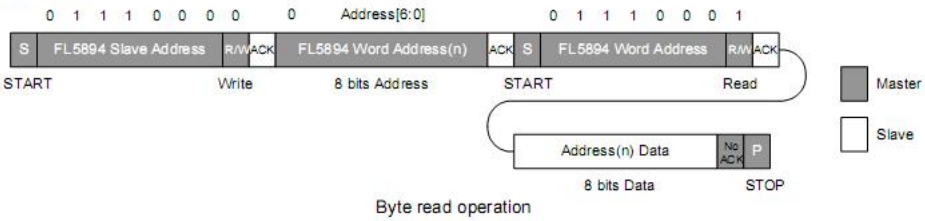
Byte write operation

During Byte write mode, the master device can give 8bit more data value. The FL5894 will increase address automatically to load data into internal register.



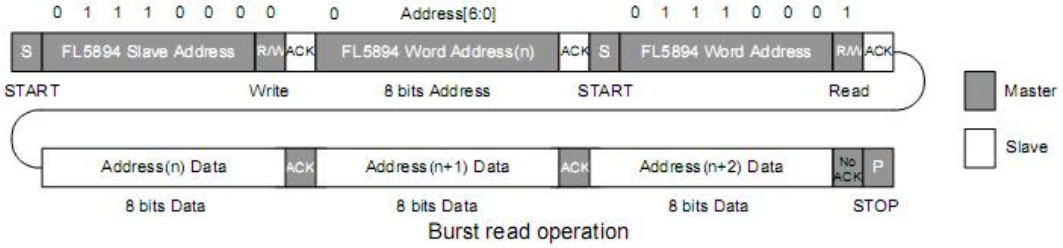
Burst write operation

The master device sends the START signal, the 7bit slave address "0111000," and the R/W=0 bit to inform the FL5894 that master device is going to do the write operation, and then the FL5894 will reply the first acknowledgement. After that, the master device sends 8-bit address to select which internal register to be read. The FL5894 reply the second acknowledgement if the register address is valid. Instead of the STOP signal, the master device sends another START signal, the 7bit slave address "0111000," and the R/W=1 bit to inform the FL5894 that the master device is going to do the READ operation, and the FL5894 will reply both the third acknowledgement and 8-bit data of the internal register value. Then the master device sends a not acknowledgement of read data, and the STOP signal.



Byte read operation

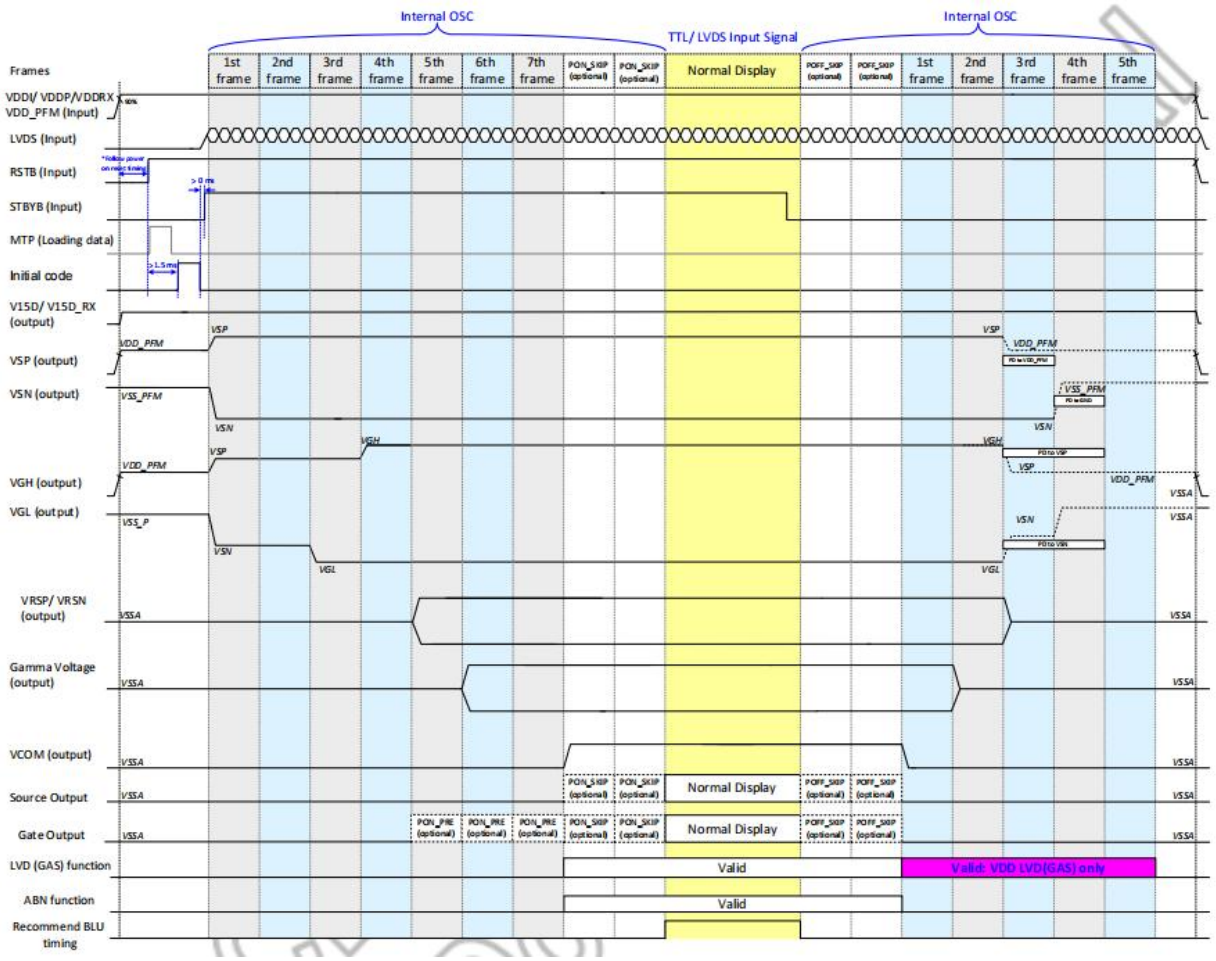
When the master device receives data from the FL5894 and sends an acknowledgement, the FL5894 will reply data until the FL5894 receives a *not* acknowledgement.



Burst read operation

Note: 4.7K~8Kohm Pull-High resistance was suggested. (Only I2C_SDA signal needs).

9.4. Power ON/OFF Sequence



10. Quality Assurance

10.1. Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

10.2. Standard for Quality Test

10.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

10.2.2. Sampling Criteria:

Visual inspection: AQL 1.5

Electrical functional: AQL 0.65.

10.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

10.3. Nonconforming Analysis & Disposition

10.3.1. Nonconforming analysis:

10.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

10.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

10.3.1.3. If cannot finish the analysis on time, customer will be notified with the progress status.

10.3.2. Disposition of nonconforming:

10.3.2.1. Non-conforming product over PPM level will be replaced.

10.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

10.4. Agreement Items

Shall negotiate with customer if the following situation occurs:

10.4.1. There is any discrepancy in standard of quality assurance.

10.4.2. Additional requirement to be added in product specification.

10.4.3. Any other special problem.

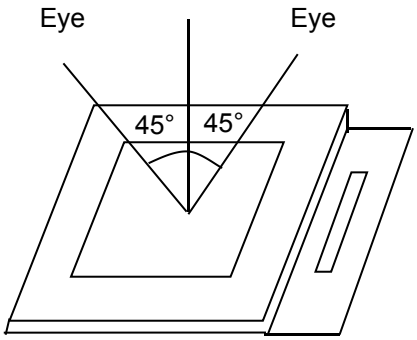
10.5. Standard of the Product Visual Inspection

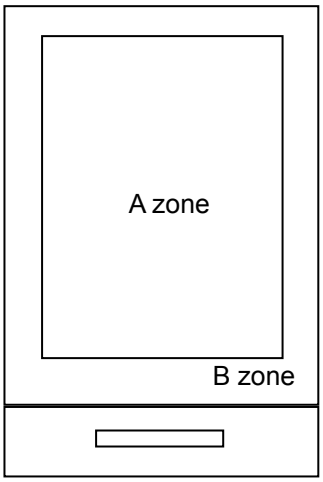
10.5.1. Appearance inspection:

10.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

10.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

10.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,



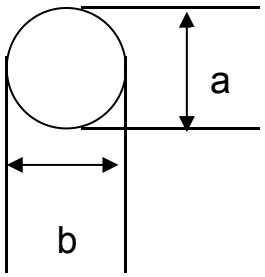


10.5.2. Basic principle:

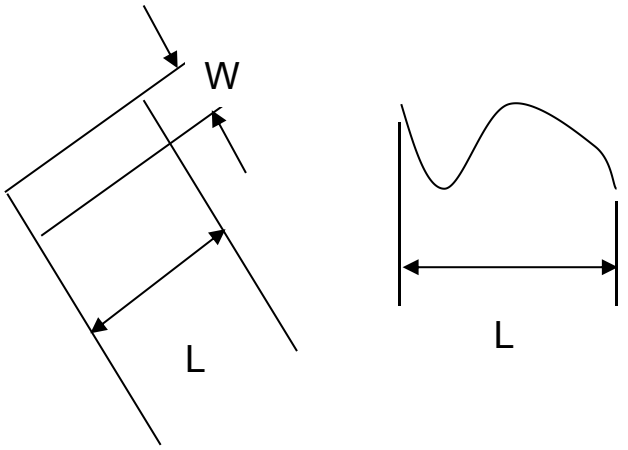
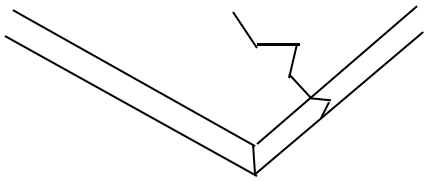
10.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

10.5.2.2. New item must be added on time when it is necessary.

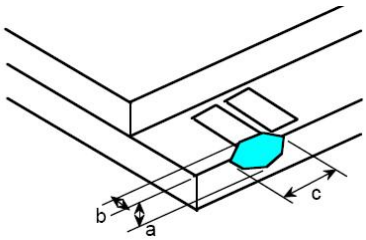
10.6. Inspection Specification

<table>
<tr><th>No.</th><th>Item</th><th>Criteria (Unit: mm)</th></tr>
<tr><td>01</td><td>Black / White spot
Foreign material
(Round type)
Pinholes
Stain
Particles inside cell.
(Minor defect)</td><td>


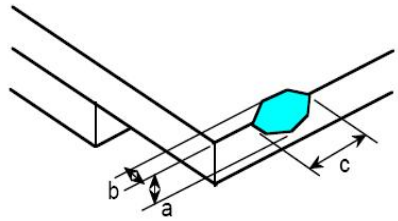
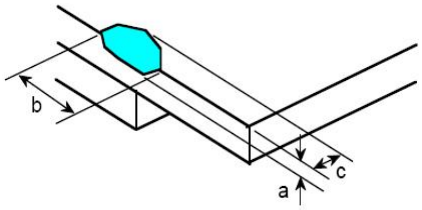
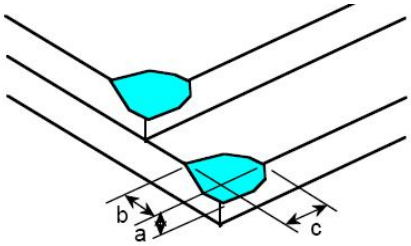
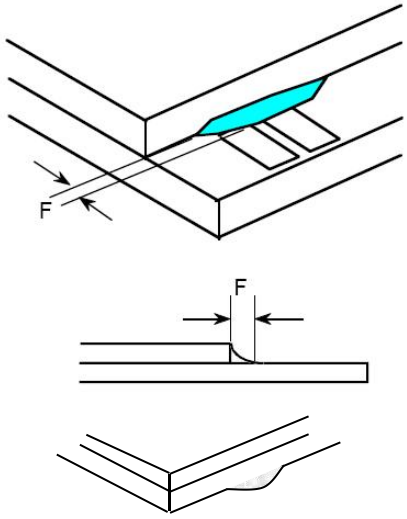
<table>
<tr><th>Area / Size</th><th>Acc. Qty</th></tr>
<tr><td>φ≤0.20</td><td>Ignore</td></tr>
<tr><td>0.20<φ≤0.50</td><td>N≤3</td></tr>
<tr><td>0.50<φ</td><td>0</td></tr>
</table>
φ= (a + b) /2
Distance between 2 defects should more than 3mm apart.
</td></tr>
<tr><td>02</td><td>Electrical Defect
(Minor defect)</td><td>
<table>
<tr><td></td><td>Display Area</td><td>Total</td><td rowspan="4">Note1</td></tr>
<tr><td>Bright dot</td><td>N⩽2</td><td>N⩽2</td></tr>
<tr><td>Dark dot</td><td>N⩽4</td><td>N⩽4</td></tr>
<tr><td>Total dot</td><td>N⩽4</td><td>N⩽4</td></tr>
<tr><td>Mura</td><td colspan="2">Not visible through 5% ND filters.</td><td>Note 2</td></tr>
</table>
Remark:
1. Bright dot caused by scratch and foreign object accords to item 1.
</td></tr>
</table>

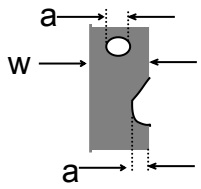
03	Black and White line Scratch Foreign material (Line type) (Minor defect)	 Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.
04	Glass Crack (Minor defect)	 Crack is potential to enlarge, any type is not allowed.

Length	Width	Acc. Qty
/	W ≦ 0.03	Ignore
L ≦ 2.5	0.03 ＜ W ≦ 0.05	3
L ≦ 2.5	0.05 ＜ W ≦ 0.10	2
/	0.1 ＜ W	0
Total		3

05	Glass Chipping Pad Area: (Minor defect) 	

Length and Width	Acc. Qty
c > 3.0, b< 1.0	1
c< 3.0, b< 1.0	3
a<Glass Thickness	

<table>
<tr>
<td>06</td>
<td>Glass Chipping Rear of Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>07</td>
<td>Glass Chipping Except Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>08</td>
<td>Glass Corner Chipping:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c < 3.0, b< 3.0</td><td>Ignore</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>09</td>
<td>Glass Burr:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length</th><th>Acc. Qty</th></tr>
<tr><td>F < 1.0</td><td>Ignore</td></tr>
</table>
Glass burr don’t affect assemble and module dimension.</td>
</tr>
</table>

<table>
<tr><td>10</td><td>FPC Defect:
(Minor defect)
  </td><td>10.1 Dent, pinhole width a<w/3.
(w: circuitry width.)
10.2 Open circuit is unacceptable.
10.3 No oxidation, contamination and distortion.</td></tr>
<tr><td>11</td><td>Bubble on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 <φ≤0.50</td><td>1</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>12</td><td>Dent on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 <φ≤0.50</td><td>1</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>13</td><td>Bezel</td><td>13.1 No rust, distortion on the Bezel.
13.2 No visible fingerprints, stains or other contamination.</td></tr>
<tr><td>14</td><td>PCB</td><td>14.1 No distortion or contamination on PCB terminals.
14.2 All components on PCB must same as documented on the BOM/component layout.
14.3 Follow IPC-A-600F.</td></tr>
<tr><td>15</td><td>Soldering</td><td>Follow IPC-A-610C standard</td></tr>
<tr><td>16</td><td>Electrical Defect
(Major defect)</td><td>The below defects must be rejected.
16.1 Missing vertical / horizontal segment,
16.2 Abnormal Display.
16.3 No function or no display.
16.4 Current exceeds product specifications.
16.5 LCD viewing angle defect.
16.6 No Backlight.
16.7 Dark Backlight.
16.8 Touch Panel no function.</td></tr>
</table>

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

10.7. Classification of Defects

10.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

10.7.2. Two minor defects are equal to one major in lot sampling inspection.

10.8. Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

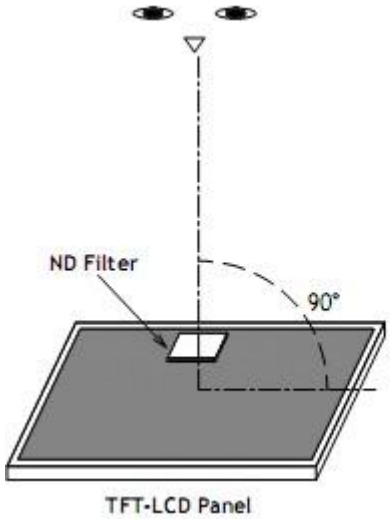
10.9. Packing

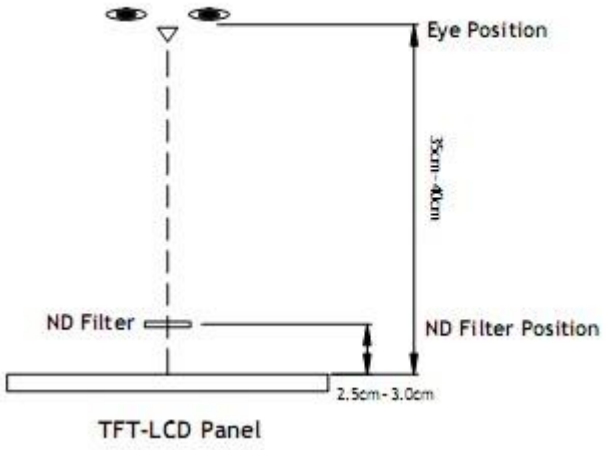
10.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

10.9.2. Modules inside package box should have compliant mark.

10.9.3. All direct package materials shall offer ESD protection.

Note1: Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.





Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

11. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	**70℃, 96Hrs**	2	GB/T2423.2 -2008
2	Low Temperature Operating	**-20℃, 96Hrs**	2	GB/T2423.1 -2008
3	High Humidity Storage	**50℃, 90%RH, 96Hrs**	2	GB/T2423.3 -2016
4	High Temperature Storage	**80℃, 96Hrs**	2	GB/T2423.2 -2008
5	Low Temperature Storage	**-30℃, 96Hrs**	2	GB/T2423.1 -2008
6	Thermal Cycling Test Storage	**-20℃, 60min ~ 70℃, 60min, 20 cycles.**	2	GB/T2423.22 -2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 30 min for each direction.	-	GB/T5170.14 -2009
8	Electrical Static Discharge	Air:±4KV 150pF/330Ω 5 times Contact:±2KV 150pF/330Ω 5 times	2	GB/T17626.2 -2018
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	-	GB/T2423.8 -1995

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

12. Precautions and Warranty

12.1. Safety

12.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

12.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

12.2. Handling

12.2.1. Reverse and use within ratings in order to keep performance and prevent damage.

12.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

12.3. Storage

12.3.1. Do not store the LCD module beyond the specified temperature ranges.

12.3.2. Strong light exposure causes degradation of polarizer and color filter.

12.4. Metal Pin (Apply to Products with Metal Pins)

12.4.1. Pins of LCD and Backlight

12.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

12.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

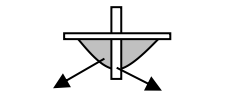
Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

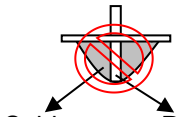
Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

12.4.1.3. Solder Wetting



Recommended



Not Recommended

12.4.2. Pins of EL

12.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

12.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

12.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270～290℃

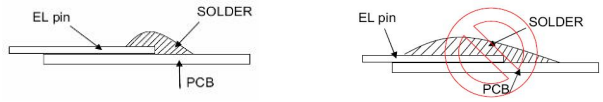
Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

12.4.2.4. No horizontal press on the EL leads during soldering.

12.4.2.5. 180° bend EL leads three times is not allowed.

12.4.2.6. Solder Wetting

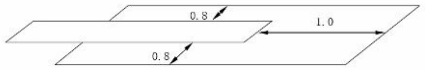


Recommended Not Recommended

12.4.2.7. The type of the solder iron:

Recommended Not Recommended

12.4.2.8. Solder Pad



12.5. Operation

12.5.1. Do not drive LCD with DC voltage

12.5.2. Response time will increase below lower temperature

12.5.3. Display may change color with different temperature

12.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

12.5.5. Do not connect or disconnect the LCM to or from the system when power is on.

12.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.

12.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

12.5.8. Do not display the fixed pattern for long time（we suggest the time not longer than one hour）because it will develop image sticking due to the TFT structure.

12.6. Static Electricity

12.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

12.6.2. The normal static prevention measures should be observed for work clothes and benches.

12.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

12.7. Limited Warranty

12.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

12.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

12.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

13. Packaging

TBD

14. Outline Drawing