PRODUCT SPECIFICATION

4.0” TFT LCD MODULE
MODEL: YDP LCD I 400 SRM

ROHS

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY
TFT S. G. H 20220816	———	———	TFT C. L 20220816

knitter-switch

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2022.08.16	CL	Initial Release	

Table of Contents

1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	4.0”	
LCD type	IPS TFT	
Display Mode	Transmissive /Normally Black	
Resolution	400 RGB x 960	Pixels
View Direction	Full viewing	Best Image
Module Outline	42.9(H) x 102.08(V) x 2.15(T) (Note1)	mm
Active Area	39.18(H) x94.03(V)	mm
Pixel Pitch	97.95(H) x 97.95(V)	um
Pixel Arrangement	RGB Vertical stripe	
Polarizer Type	Glare	
Display Colors	16.7M	
Interface	3/4 wire SPI 16/18/24bit RGB Interface MIPI Interface	
Driver IC	ST7701SI	
With or without the touch panel	Without	
Operating Temperature	**-20～70**	ºC
Storage Temperature	**-30～80**	ºC
Weight	20	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

GND=0V, Ta=25ºC

Item	Symbol	Min.	Max.	Unit
Supply Voltage	VCC	-0.3	4.6	V
Storage temperature	T_{STG}	**-30**	**+80**	ºC
Operating temperature	T_{OP}	**-20**	**+70**	ºC

Note 1: If Ta below 50ºC, the maximal humidity is 90%RH, if Ta over 50ºC, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCC	2.5	2.8	3.3	V
Logic Low input voltage	V_{IL}	GND	-	0.3*VCC	V
Logic High input voltage	V_{IH}	0.7*VCC	-	VCC	V
Logic Low output voltage	V_{OL}	GND	-	0.2*VCC	V
Logic High output voltage	V_{OH}	0.8*VCC	-	VCC	V
Current Consumption All White	I_{VCCA}	-	30	-	mA

5. Backlight Characteristic

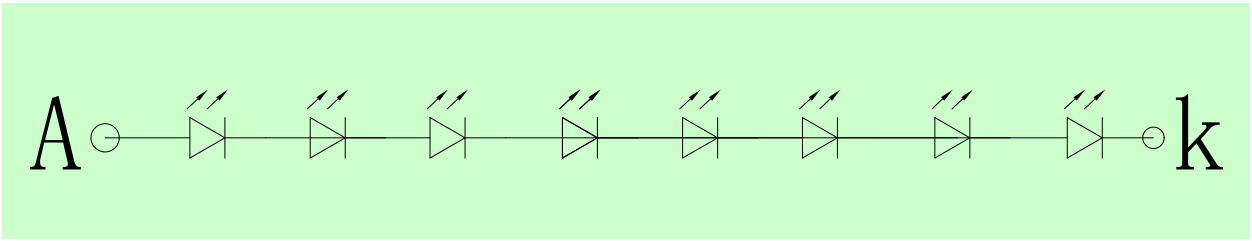
5.1. Backlight Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V_F	Ta=25 ºC, I_F=20mA/LED	22.4	**24.8**	27.2	V
Forward Current	I_F	Ta=25 ºC, V_F=3.1V/LED	-	**20**	-	mA
Power dissipation	P_D	-	-	**496**	-	mW
Uniformity	Avg	-	-	80	-	%
LED working life(25℃)			-	30000	-	Hrs
Drive method	**Constant current**					
LED Configuration	8 White LEDs (8 LEDs in one string)					

Note1: LED life time defined as follows: The final brightness is at 50% of original brightness.

The environmental conducted under ambient air flow, at Ta=25±2 ºC,60%RH±5%, I_F=20mA/LED.

5.2. Backlighting circuit



6. Optical Characteristics

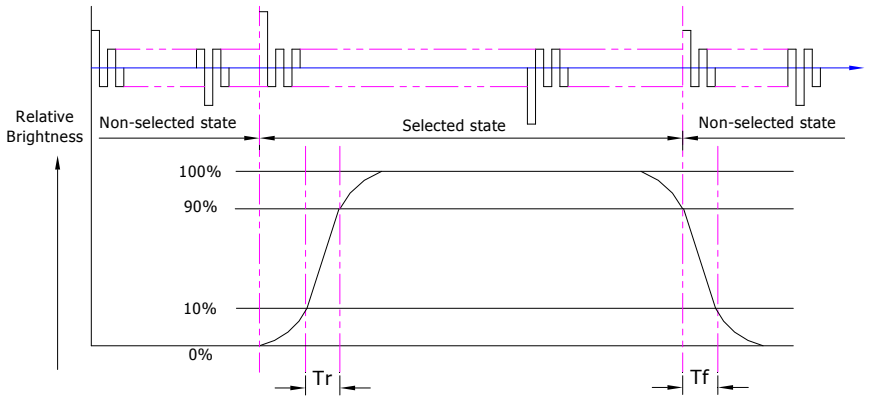
6.1. Optical Characteristics

Ta=25ºC, VCC=2.8V

	Item		Symbol	Condition	Specification			Unit
					Min.	Typ.	Max.	
Backlight On (Transmissive Mode)	Luminance on TFT(I_f =20mA)		Lv	Normally viewing angle θX = φY =0º	**240**	**300**	-	cd/m²
	Contrast ratio(See 6.3)		CR		1000	1500	-	
	Response time (See 6.2)		TR+TF		-	30	40	ms
	Chromaticity Transmissive (See6.5)	Red	XR		**0.585**	**0.635**	**0.685**	
			YR		**0.258**	**0.308**	**0.358**	
		Green	XG		**0.249**	**0.299**	**0.349**	
			YG		**0.533**	**0.583**	**0.633**	
		Blue	XB		**0.084**	**0.134**	**0.184**	
			YB		**0.014**	**0.064**	**0.114**	
		White	XW		**0.221**	**0.271**	**0.321**	
			YW		**0.246**	**0.296**	**0.346**	
	Viewing Angle (See 6.4)	Horizontal	θX+	Center CR≥10	**80**	**85**	-	Deg.
			θX-		**80**	**85**	-	
		Vertical	φY+		**80**	**85**	-	
			φY-		**80**	**85**	-	
	NTSC Ratio(Gamut)				60	65	-	%

6.2. Definition of Response Time

6.2.1. Normally Black Type (Negative)

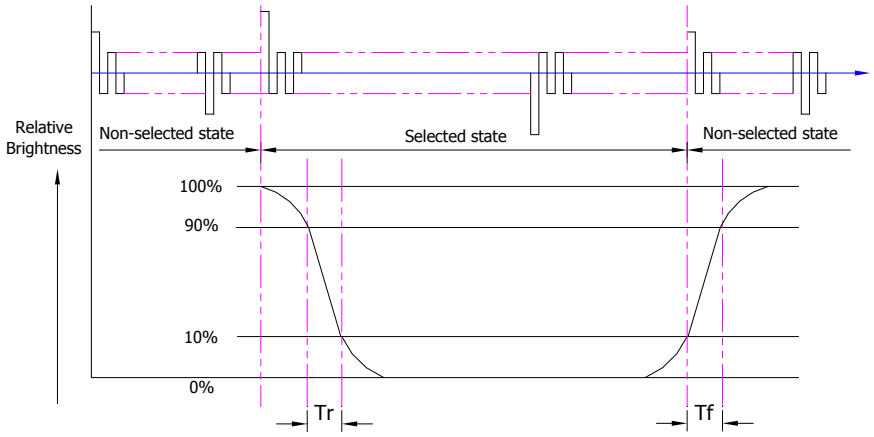


Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note: Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)



Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note: Measuring machine: LCD-5100 or EQUI

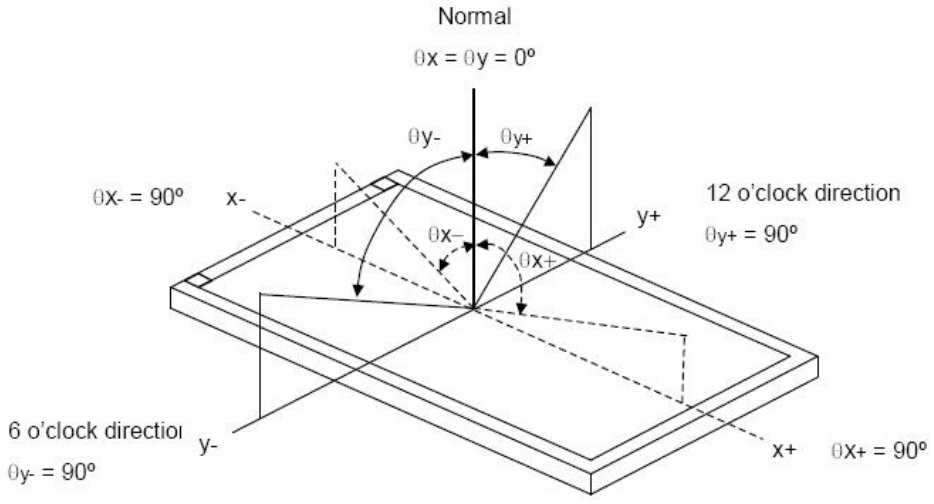
6.3. Definition of Contrast Ratio

Contrast is measured perpendicular to display surface in reflective and transmissive mode. The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

6.4. Definition of Viewing Angles



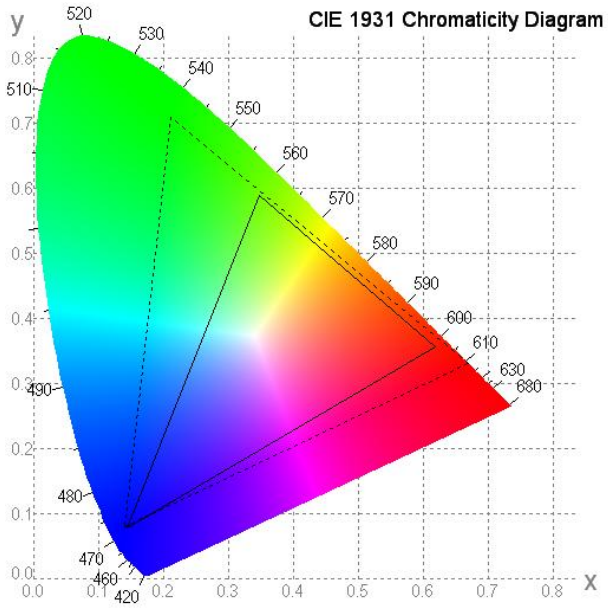
Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



6.6. Definition of Surface Luminance, Uniformity and Transmittance

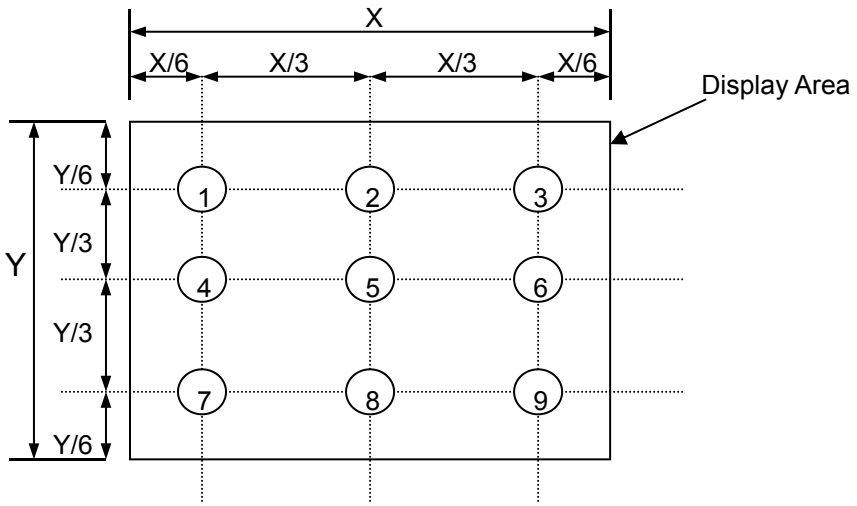
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1. Surface Luminance: L_V = average (L_{P1}:L_{P9})

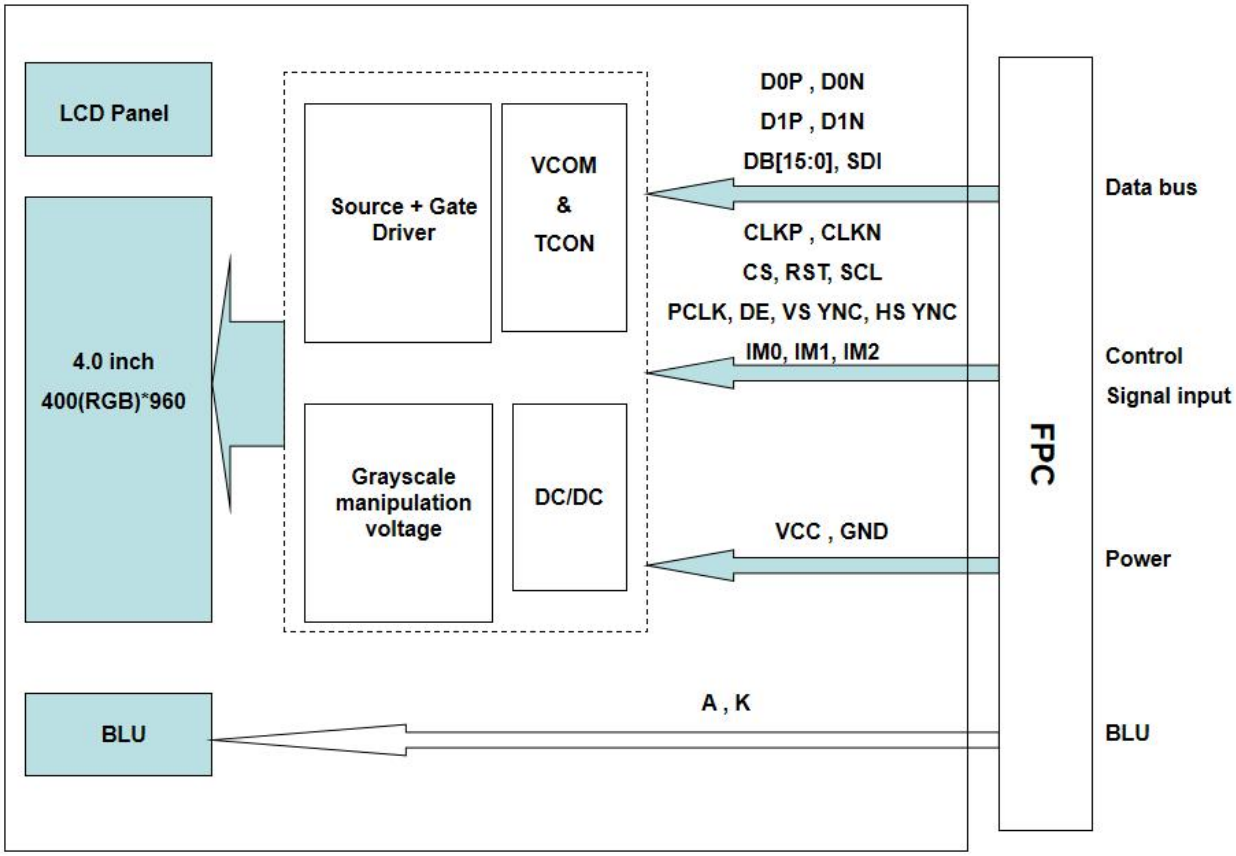
6.6.2. Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%

6.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note: Measuring machine: BM-7



7. Block Diagram and Power Supply



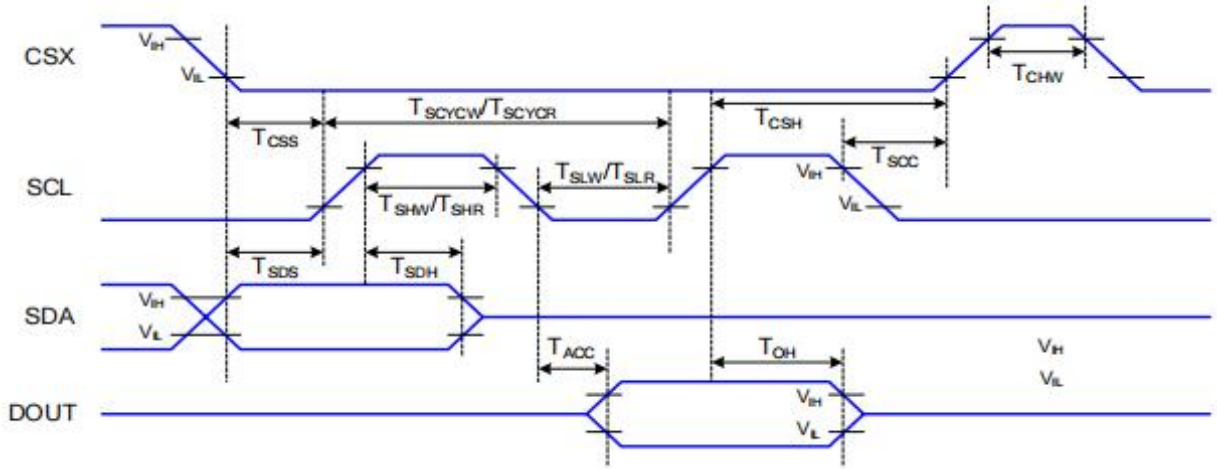
8. Interface Pins Definition

No.	Symbol	Function
1	A	Anode for back light driver voltage
2	K	Cathode for back light driver voltage
3	VCC	Power supply
4	GND	Ground
5	D0N	MIPI DSI differential data pair
6	D0P	MIPI DSI differential data pair
7	GND	Ground
8	CLKN	MIPI DSI differential clock pair
9	CLKP	MIPI DSI differential clock pair
10	GND	Ground
11	D1N	MIPI DSI differential data pair
12	D1P	MIPI DSI differential data pair
13	GND	Ground
14	VS YNC	Frame synchronizing signal
15	HS YNC	Line synchronizing signal
16	PCLK	Clock signal to sample each data
17	DE	Input data enable control
18	DB0	Data bus
19	DB1	Data bus
20	DB2	Data bus
21	DB3	Data bus
22	DB4	Data bus
23	DB5	Data bus
24	DB6	Data bus
25	DB7	Data bus
26	DB8	Data bus
27	DB9	Data bus
28	DB10	Data bus
29	DB11	Data bus
30	DB12	Data bus
31	DB13	Data bus
32	DB14	Data bus
33	DB15	Data bus
34	RESET	The external reset input
35	CS	A chip select signal.
36	SCL	Serial clock
37	SDI	Serial data input pin for SPI Interface

<table>
<tr><td>38</td><td>IM2</td><td rowspan="3">Select the MPU system interface mode:
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface mode</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RGB+8b_SPI(fall)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>RGB+9b_SPI(fall)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>RGB+16b_SPI(rise)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MIPI</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI+16b_SPI(rise)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RGB+8b SPI(rise)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>RGB+9b SPI(rise)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>RGB+16b SPI(fall)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI+16b_SPI(fall)</td></tr>
</table></td></tr>
<tr><td>39</td><td>IM1</td></tr>
<tr><td>40</td><td>IM0</td></tr>
</table>

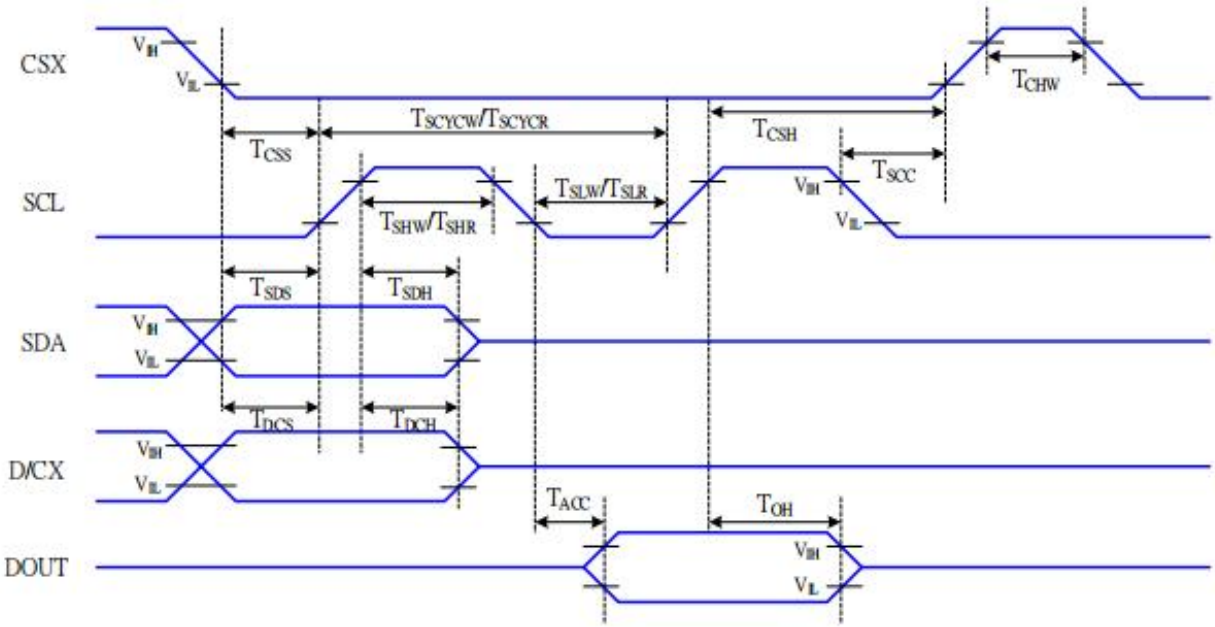
9. AC Characteristics

9.1. Serial Interface Characteristics (3-line serial)



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

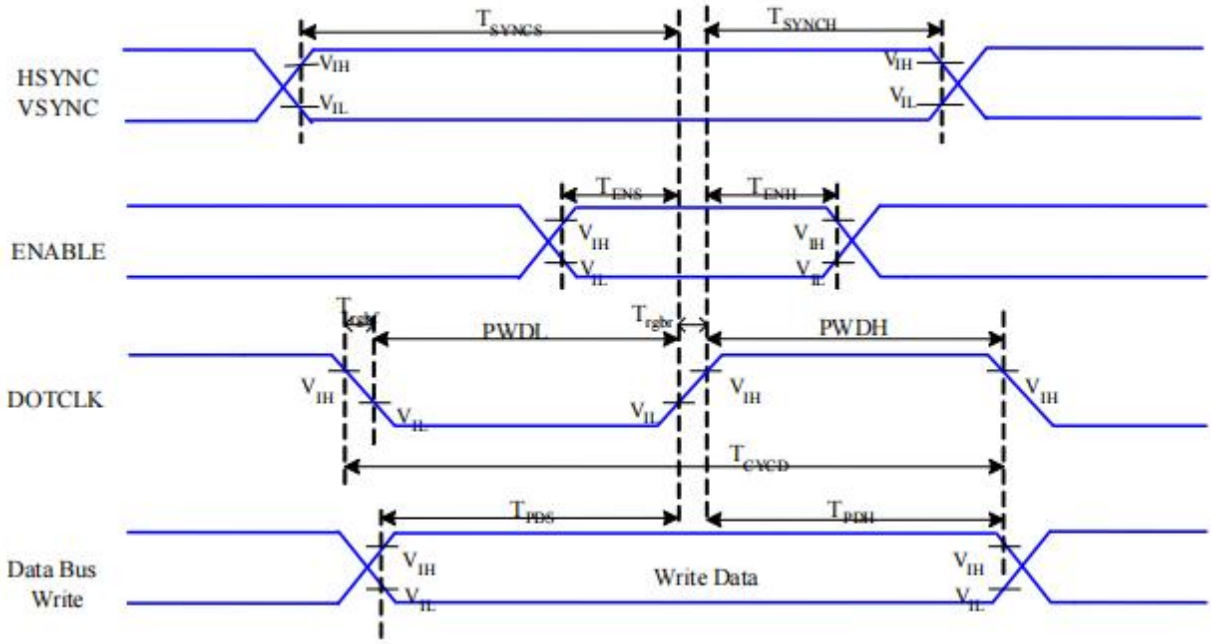
9.2. Serial Interface Characteristics (4-line serial)



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

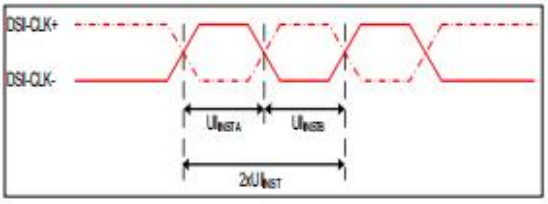
9.3. RGB Interface Characteristics

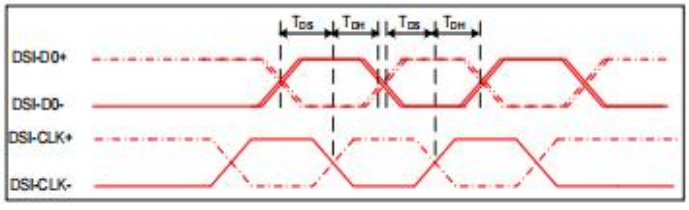


Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

9.4. MIPI Interface Characteristics

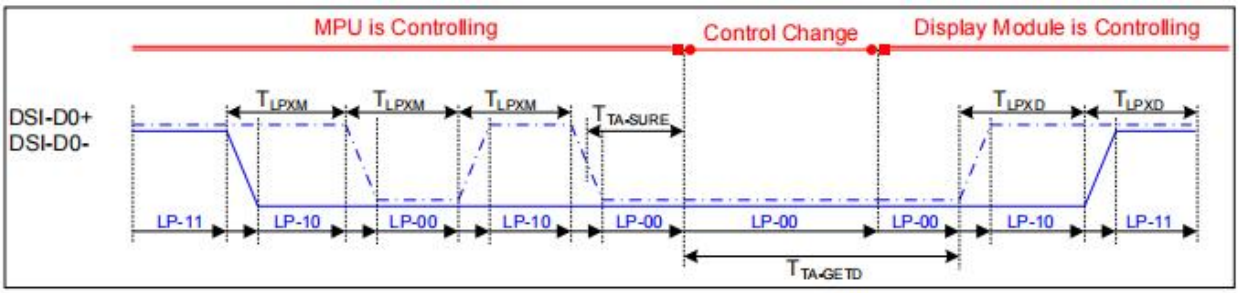
High Speed Mode:

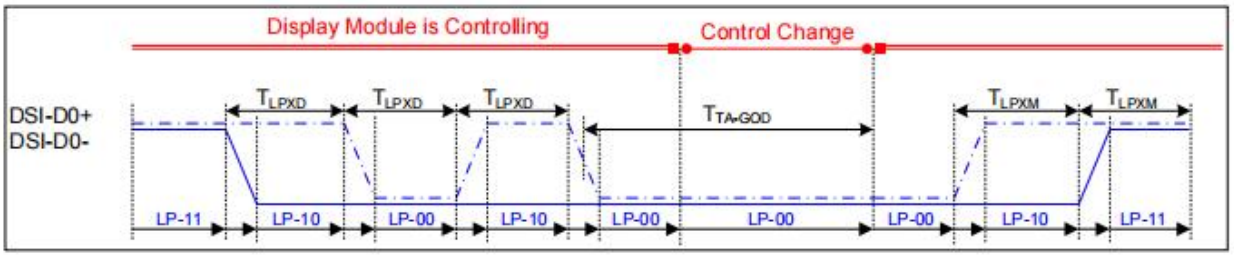




Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	2.5	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	1.25	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

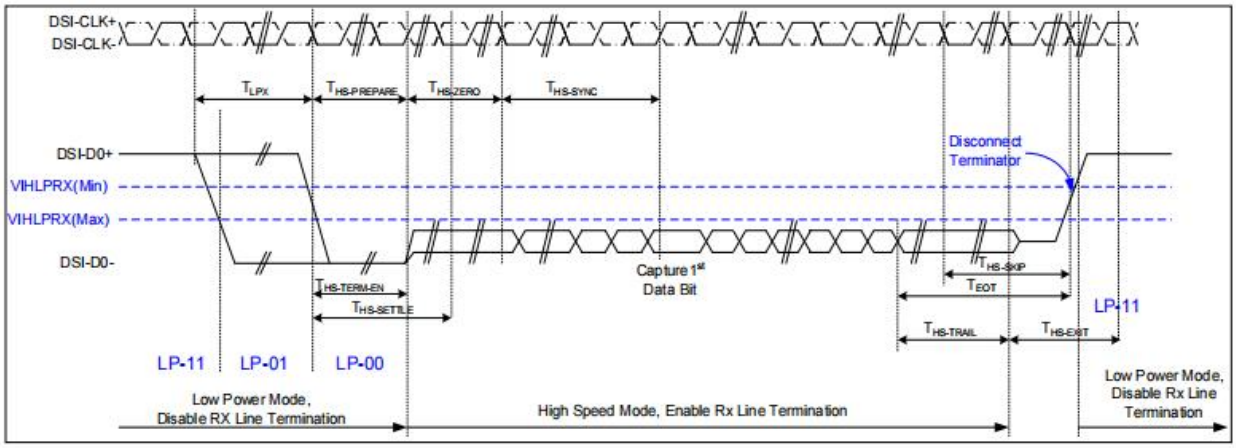
Lowe Power Mode :

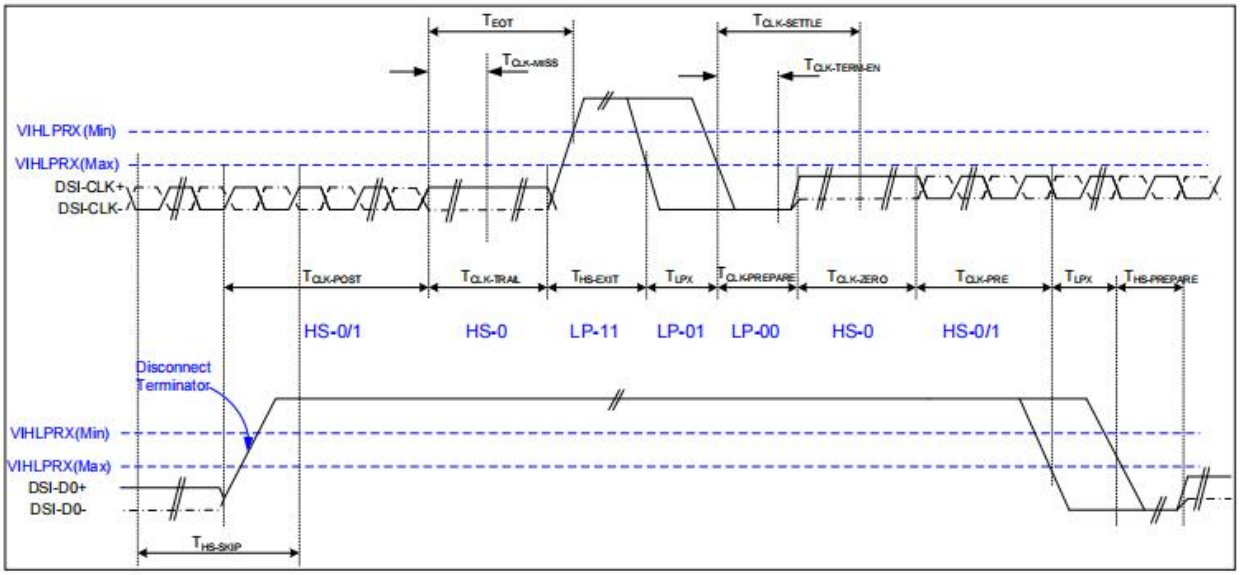




Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

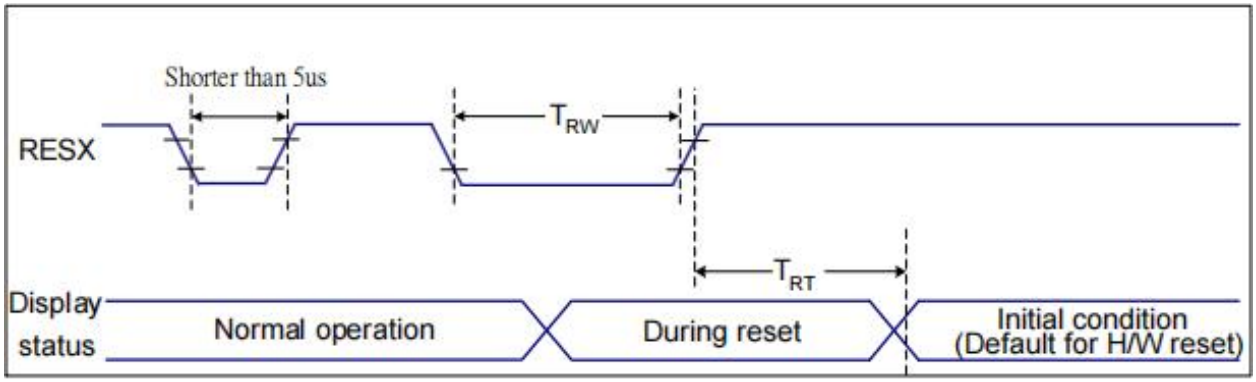
DSI Bursts Mode:





Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

10. Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

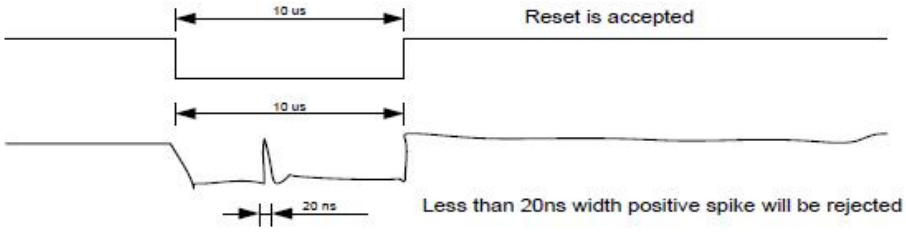
Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 42.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

11. Quality Assurance

11.1. Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

11.2. Standard for Quality Test

11.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

11.2.2. Sampling Criteria:

Visual inspection: AQL 1.5

Electrical functional: AQL 0.65.

11.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

11.3. Nonconforming Analysis & Disposition

11.3.1. Nonconforming analysis:

11.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

11.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

11.3.1.3. If can not finish the analysis on time, customer will be notified with the progress status.

11.3.2. Disposition of nonconforming:

11.3.2.1. Non-conforming product over PPM level will be replaced.

11.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

11.4. Agreement Items

Shall negotiate with customer if the following situation occurs:

11.4.1. There is any discrepancy in standard of quality assurance.

11.4.2. Additional requirement to be added in product specification.

11.4.3. Any other special problem.

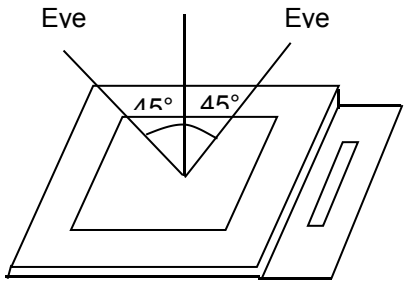
11.5. Standard of the Product Visual Inspection

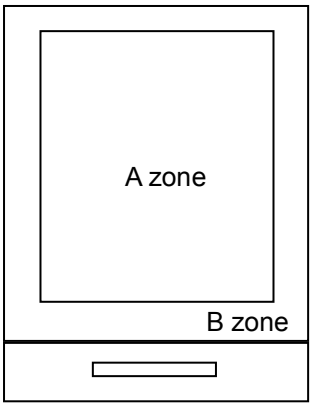
11.5.1. Appearance inspection:

11.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

11.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

11.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,



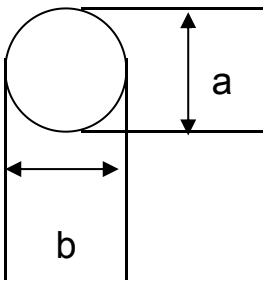


11.5.2. Basic principle:

11.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

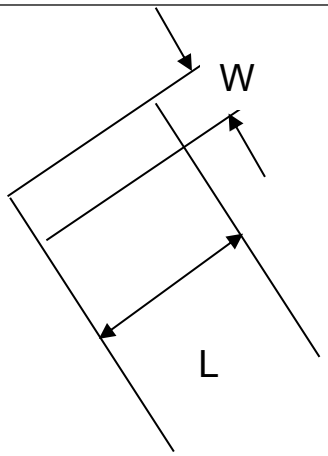
11.5.2.2. New item must be added on time when it is necessary.

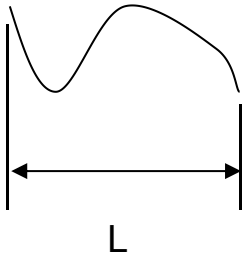
11.6. Inspection Specification

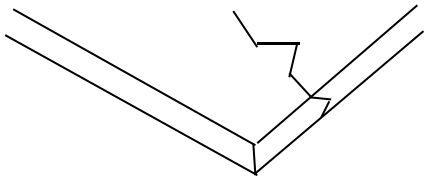
<table>
<tr><th>No.</th><th>Item</th><th>Criteria (Unit: mm)</th></tr>
<tr><td>01</td><td>Black / White spot
Foreign material
(Round type)
Pinholes
Stain
Particles inside cell.
(Minor defect)</td><td>


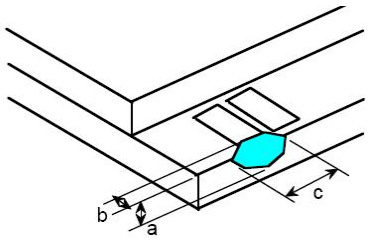
<table>
<tr><th>Area / Size</th><th>Acc. Qty</th></tr>
<tr><td>φ≤0.10</td><td>Ignore</td></tr>
<tr><td>0.10<φ≤0.15</td><td>2</td></tr>
<tr><td>0.15<φ≤0.25</td><td>1</td></tr>
<tr><td>0.25<φ</td><td>0</td></tr>
<tr><td>Total</td><td>2 no include φ≤ 0.10</td></tr>
</table>
φ= (a + b) /2

Distance between 2 defects should more than 3mm apart.
</td></tr>
<tr><td>02</td><td>Electrical Defect
(Minor defect)</td><td>
<table>
<tr><td></td><td>Display Area</td><td>Total</td><td rowspan="4">Note1</td></tr>
<tr><td>Bright dot</td><td>0</td><td>0</td></tr>
<tr><td>Dark dot</td><td>N≤2</td><td>N≤2</td></tr>
<tr><td>Total dot</td><td>N≤2</td><td>N≤2</td></tr>
<tr><td>Mura</td><td colspan="2">Not visible through 5% ND filters.</td><td>Note2</td></tr>
</table>
Remark:
1. Bright dot caused by scratch and foreign object accords to item 1.
</td></tr>
</table>

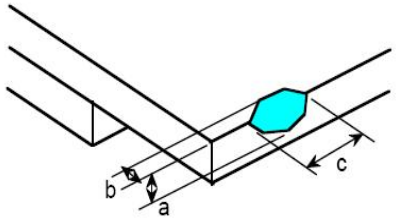
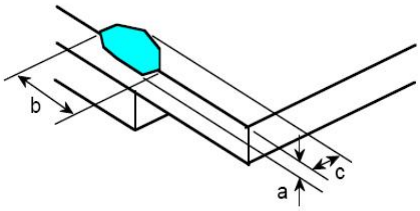
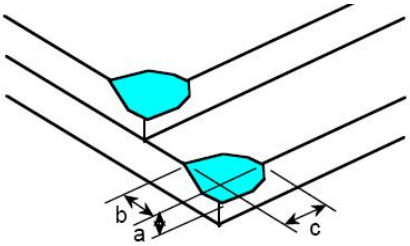
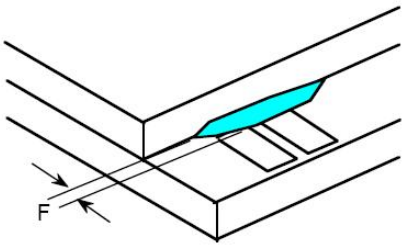
<table>
<tr>
<td>03</td>
<td>Black and White line
Scratch
Foreign material
(Line type)
(Minor defect)</td>
<td>


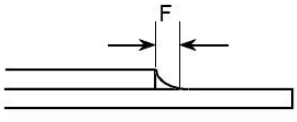


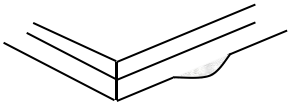
<table>
<tr><th>Length</th><th>Width</th><th>Acc. Qty</th></tr>
<tr><td>/</td><td>W ≦ 0.03</td><td>Ignore</td></tr>
<tr><td>L ≦ 2.5</td><td>0.03 ＜ W ≦ 0.05</td><td>3</td></tr>
<tr><td>L ≦ 2.5</td><td>0.05 ＜ W ≦ 0.10</td><td>2</td></tr>
<tr><td>/</td><td>0.1 ＜ W</td><td></td></tr>
<tr><td colspan="2">Total</td><td>3</td></tr>
</table>
Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.
</td>
</tr>
<tr>
<td>04</td>
<td>Glass Crack
(Minor defect)</td>
<td>

Crack is potential to enlarge, any type is not allowed.
</td>
</tr>
</table>

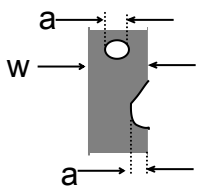
<table>
<tr>
<td>05</td>
<td>Glass Chipping Pad Area:
(Minor defect)


</td>
<td>
<table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>3</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table>
</td>
</tr>
<tr>
<td>06</td>
<td>Glass Chipping Rear of Pad Area:
(Minor defect)</td>
<td>
<table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr><td></td><td> 
</td><td></td></tr>
<tr><td>07</td><td>Glass Chipping Except Pad Area:
(Minor defect)
 
</td><td><table>
<tr><td>Length and Width</td><td>Acc. Qty</td></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td></tr>
<tr><td>08</td><td>Glass Corner Chipping:
(Minor defect)
 
</td><td><table>
<tr><td>Length and Width</td><td>Acc. Qty</td></tr>
<tr><td>c < 3.0, b< 3.0</td><td>Ignore</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td></tr>
<tr><td>09</td><td>Glass Burr:
(Minor defect)
 

  </td><td><table>
<tr><td>Length</td><td>Acc. Qty</td></tr>
<tr><td>F < 1.0</td><td>Ignore</td></tr>
</table>
Glass burr don’t affect assemble and module dimension.</td></tr>
</table>

<table>
<tr><td>10</td><td>FPC Defect:
(Minor defect)
  </td><td>10.1 Dent, pinhole width a<w/3.
(w: circuitry width.)
10.2 Open circuit is unacceptable.
10.3 No oxidation, contamination and distortion.</td></tr>
<tr><td>11</td><td>Bubble on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 <φ≤0.50</td><td>1</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>12</td><td>Dent on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 <φ≤0.50</td><td>1</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>13</td><td>Bezel</td><td>13.1 No rust, distortion on the Bezel.
13.2 No visible fingerprints, stains or other contamination.</td></tr>
<tr><td>14</td><td>PCB</td><td>14.1 No distortion or contamination on PCB terminals.
14.2 All components on PCB must same as documented on the BOM/component layout.
14.3 Follow IPC-A-600F.</td></tr>
<tr><td>15</td><td>Soldering</td><td>Follow IPC-A-610C standard</td></tr>
<tr><td>16</td><td>Electrical Defect
(Major defect)</td><td>The below defects must be rejected.
16.1 Missing vertical / horizontal segment,
16.2 Abnormal Display.
16.3 No function or no display.
16.4 Current exceeds product specifications.
16.5 LCD viewing angle defect.
16.6 No Backlight.
16.7 Dark Backlight.
16.8 Touch Panel no function.</td></tr>
</table>

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

11.7. Classification of Defects

11.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

11.7.2. Two minor defects are equal to one major in lot sampling inspection.

11.8. Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

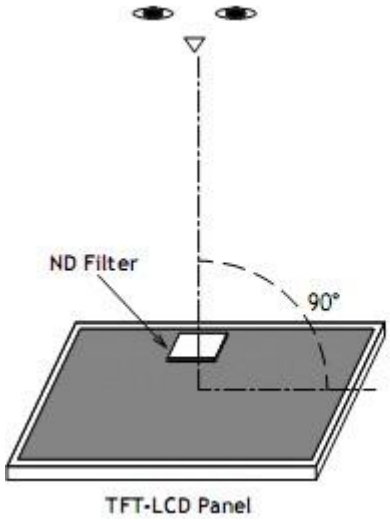
11.9. Packaging

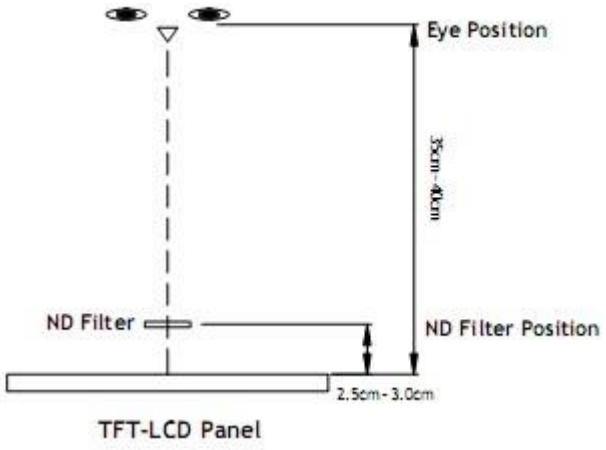
11.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

11.9.2. Modules inside package box should have compliant mark.

11.9.3. All direct package materials shall offer ESD protection.

Note1: Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.





Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

12. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	**70℃, 96Hrs**	2	GB/T2423.2 -2008
2	Low Temperature Operating	**-20℃, 96Hrs**	2	GB/T2423.1 -2008
3	High Humidity Storage	**50℃, 90%RH, 96Hrs**	2	GB/T2423.3 -2016
4	High Temperature Storage	**80℃, 96Hrs**	2	GB/T2423.2 -2008
5	Low Temperature Storage	**-30℃, 96Hrs**	2	GB/T2423.1 -2008
6	Thermal Cycling Test Storage	-20℃, 60min~ 70℃, 60min, 20 cycles.	2	GB/T2423.22 -2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 30 min for each direction.	-	GB/T5170.14 -2009
8	Electrical Static Discharge	Air:±4KV 150pF/330Ω 5 times Contact:±2KV 150pF/330Ω 5 times	2	GB/T17626.2 -2018
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	-	GB/T2423.8 -1995

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

13. Precautions and Warranty

13.1. Safety

13.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

13.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

13.2. Handling

13.2.1. Reverse and use within ratings in order to keep performance and prevent damage.

13.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

13.3. Storage

13.3.1. Do not store the LCD module beyond the specified temperature ranges.

13.3.2. Strong light exposure causes degradation of polarizer and color filter.

13.4. Metal Pin (Apply to Products with Metal Pins)

13.4.1. Pins of LCD and Backlight

13.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

13.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

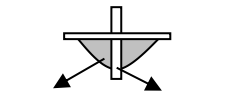
Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

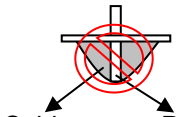
Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

13.4.1.3. Solder Wetting



Recommended



Not Recommended

13.4.2. Pins of EL

13.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

13.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

13.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270～290℃

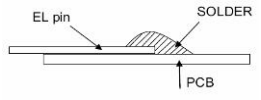
Typical Soldering Time: ≤2s

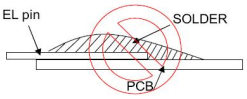
Minimum solder distance from EL lamp (body):2.0mm

13.4.2.4. No horizontal press on the EL leads during soldering.

13.4.2.5. 180° bend EL leads three times is not allowed.

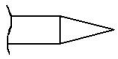
13.4.2.6. Solder Wetting

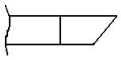




Recommended Not Recommended

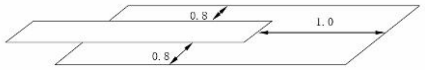
13.4.2.7. The type of the solder iron:





Recommended Not Recommended

13.4.2.8. Solder Pad



13.5. Operation

13.5.1. Do not drive LCD with DC voltage

13.5.2. Response time will increase below lower temperature

13.5.3. Display may change color with different temperature

13.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

13.5.5. Do not connect or disconnect the LCM to or from the system when power is on.

13.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.

13.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

13.5.8. Do not display the fixed pattern for long time（we suggest the time not longer than one hour）because it will develop image sticking due to the TFT structure.

13.6. Static Electricity

13.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

13.6.2. The normal static prevention measures should be observed for work clothes and benches.

13.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

13.7. Limited Warranty

13.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

13.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

13.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

14. Packaging

TBD

15. Outline Drawing