PRODUCT SPECIFICATION

15" TFT LCD MODULE
MODEL: YDP LCD I 1500 LVDS

ROHS

< ◇ >   Preliminary Specification

< ◆ >   Finally Specification

CUSTOMER'S APPROVAL	
CUSTOMER :	
SIGNATURE:	**DATE:**

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY
-	TFT S. G. H 20240921	TFT 周福云 20240921	TFT L. L 20240921

knitter-switch

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2024.09.21	LL	Initial Release	

Table of Contents

1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	15"	
LCD type	TFT IPS	
Display Mode	Transmissive /Normally black	
Resolution	1024 RGB x 768	Pixels
View Direction	full view	Best Image
Module Outline	326.6 (H) x 253.5(V) x 7.3(T) (Note1)	mm
Active Area	304.13(H) x 228.1(V)	mm
Pixel Pitch	297(H) x 297(V)	um
Pixel Arrangement	RGB Vertical stripe	
Polarizer Surface Treatment	Glare	
Display Colors	16.7M	
Driver IC	JD9168S	
Interface	LVDS	
With or without the touch panel	Without	
Operating Temperature	**-20~+70**	℃
Storage Temperature	**-20~+70**	℃
Weight	TBD	g

Note 1: Inclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

GND=0V, Ta=25℃

Item	Symbol	Min.	Max.	Unit
Supply Voltage	IOVCC	-0.3	3.6	V
Storage temperature	T_{stg}	-20	+70	℃
Operating temperature	T_{op}	-20	+70	℃

Note 1: If Ta below 50℃, the maximal humidity is 90%RH, if Ta over 50℃, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	IOVCC	2.5	-	3.3	V
Logic Low input voltage	V_{IL}	0	-	0.3*IOVCC	V
Logic High input voltage	V_{IH}	0.7*IOVCC	-	IOVCC	V
Logic Low output voltage	V_{OL}	0	-	0.2*IOVCC	V
Logic High output voltage	V_{OH}	0.8*IOVCC	-	IOVCC	V
Differential input high threshold voltage	Rx_{VTH}	+0.1	+0.2	+0.3	V
Differential input low threshold voltage	Rx_{VTL}	-0.3	-0.2	-0.1	V
Input voltage range (singled-end)	Rx_{VIN}	0.7	-	1.7	V
Differential input common mode voltage	Rx_{VCM}	1.0	1.2	1.4	V
Current Consumption All White	I_{ODD}	-	TBD	-	mA

5. Backlight Characteristic

5.1. Backlight Characteristic

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V_F	Ta=25 ℃, I_F=60mA/LED	18.2	**20.3**	22.4	V
Forward Current	I_F	Ta=25 ℃, V_F=3.0V/LED		**360**		mA
Power dissipation	P_D	-	-	**7308**	-	mW
Uniformity	Avg	-	-	80	-	%
LED working life(25℃)	-		-	30,000	-	Hrs
Drive method	Constant current					
LED Configuration	42 White LEDs (7 LEDs in one string and 2 groups in parallel)×3					

Note1：LED life time defined as follows: The final brightness is at 50% of original brightness.

The environmental conducted under ambient air flow, at Ta=25±2 ℃,60%RH±5%,I_F=60mA/LED.

5.2. Backlighting circuit
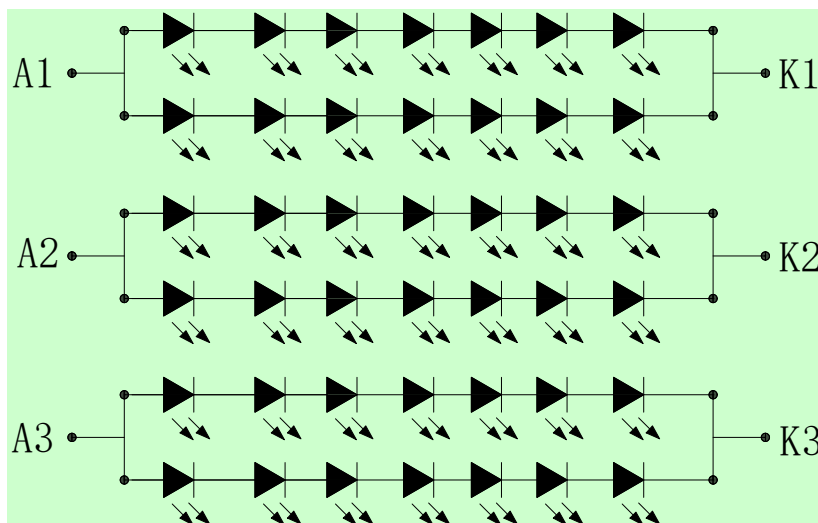
6. Optical Characteristics

6.1. Optical Characteristics

Ta=25ºC, IOVCC=3.3V

	Item		Symbol	Condition	Specification			Unit
					Min.	Typ.	Max.	
Backlight On (Transmissive Mode)	Luminance on TFT(I_f=60mA/LED)		Lv		240	300	-	cd/m²
	Contrast ratio(See 6.3)		CR		(800)	(1000)	-	
	Response time (See 6.2)		TR+TF		-	25	30	ms
	Chromaticity Transmissive (See 6.5)	Red	XR		-	TBD	-	
			YR		-	TBD	-	
		Green	XG		-	TBD	-	
			YG		-	TBD	-	
		Blue	XB		-	TBD	-	
			YB		-	TBD	-	
		White	XW		-	TBD	-	
			YW		-	TBD	-	
	Viewing Angle (See 6.4)	Horizontal	θX+	Center CR≥10	80	85	-	Deg.
			θX-		80	85	-	
		Vertical	φY+		80	85	-	
			φY-		80	85	-	
	NTSC ratio				63	67	-	%

6.2. Definition of Response Time
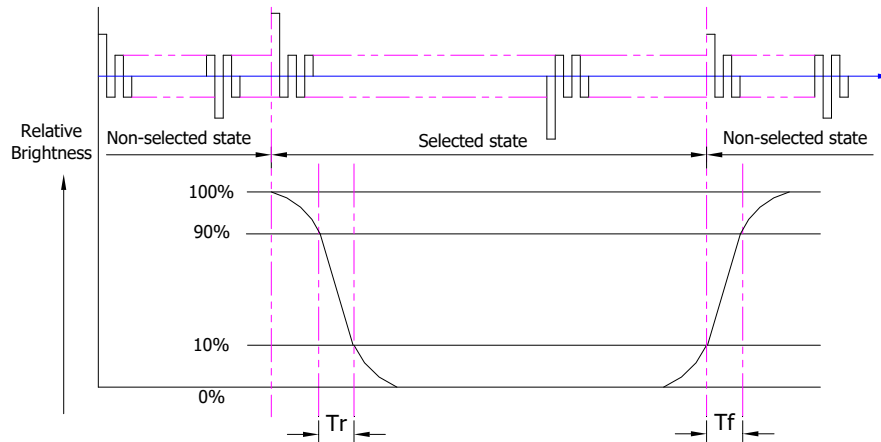
6.2.1. Normally Black Type (Negative)
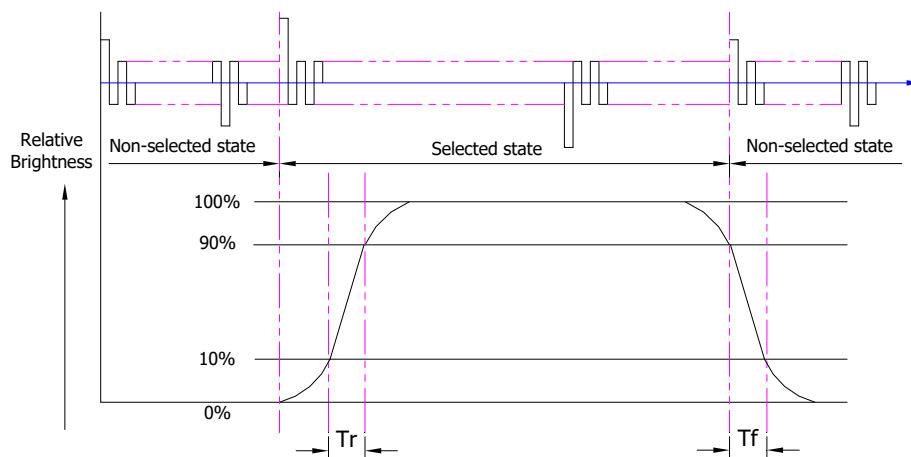
Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

6.2.2. Normally White Type (Positive)

Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note: Measuring machine: LCD-5100 or EQUI

6.3. Definition of Contrast Ratio

Contrast is measured perpendicular to display surface in reflective and transmissive mode. The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

6.4. Definition of Viewing Angles
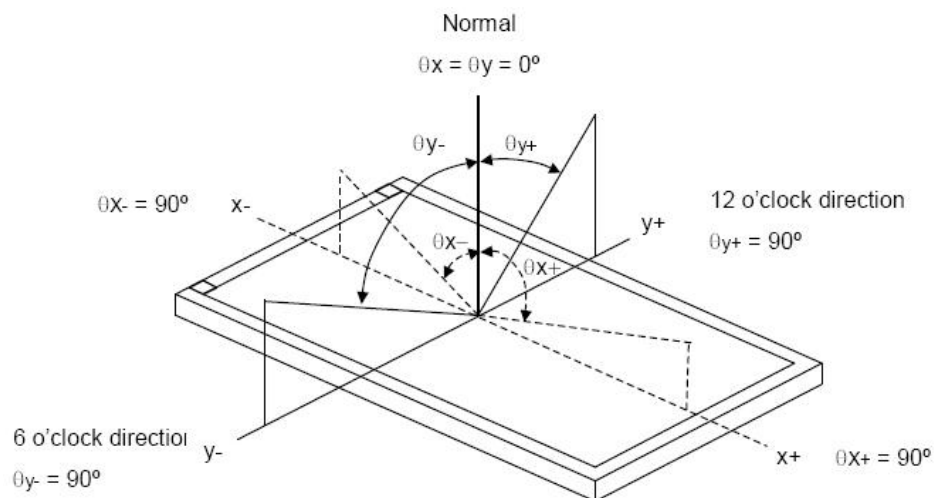
Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)

CIE 1931 Chromaticity Diagram

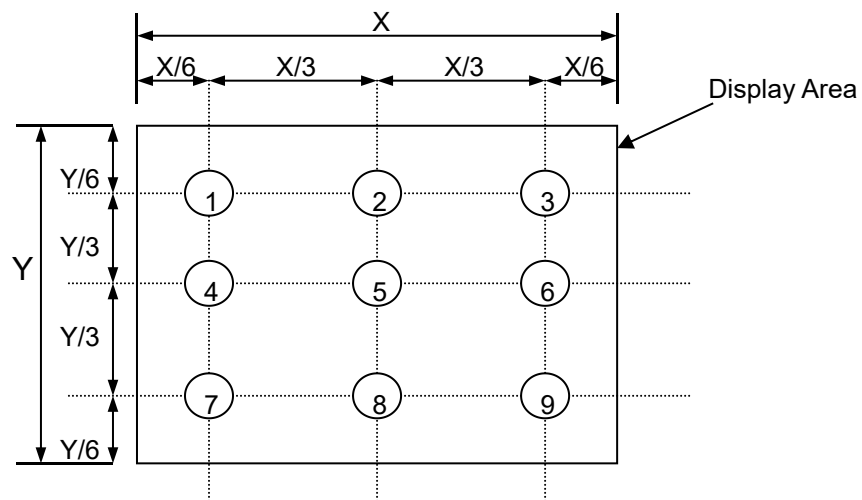## 6.6. Definition of Surface Luminance, Uniformity and Transmittance

Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

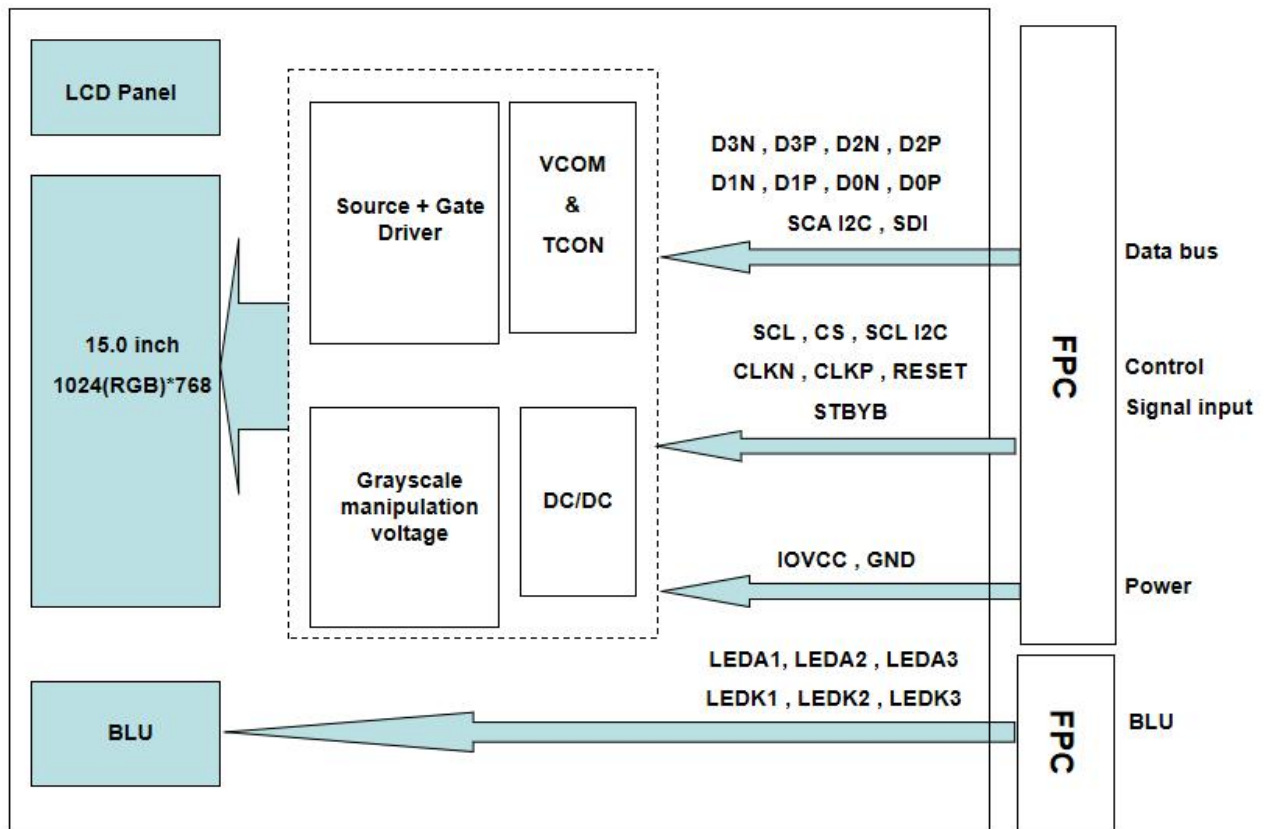6.6.1. Surface Luminance: L_V = average (L_{P1}:L_{P9})

6.6.2. Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%

6.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note: Measuring machine: BM-7

7. Block Diagram and Power Supply

8. Interface Pins Definition

No.	Symbol	Function	Remark
1	VGLO	Output voltage from the step-up circuit. Connect to a stabilizing capacitor between VGL and system ground. Place a Scotty barrier diode between AVEE and VGL. Place a Scotty barrier diode between VGL and system ground. (Optional)	
2	VGHO	Output voltage from the step-up circuit. Connect to a stabilizing capacitor between VGH and system ground. Place a Scotty barrier diode between AVDD and VGH. (Optional) The diode is needed when AVDD come from external power	
3	VSN	Input negative power from system/ external power IC	
4	VSN	Input negative power from system/ external power IC	
5	VSP	Input positive power from system/ external power IC	
6	VSP	Input positive power from system/ external power IC	
7	NC	No connection	
8	SCL	Serial clock input in SPI interface (CMDSEL=1) If not use, let it open or IOVCC or GND	
9	SDI	Serial data input / output pin in SPI interface operation (CMDSEL=1). If not use, let it open	
10	CS	Chip select pin. (CMDSEL=1) 0: Chip can be accessed; 1: Chip cannot be accessed. If this pin is not used, please connect it to IOVCC	
11	STBYB	Standby mode. | STBYB	IC Status | |---|---| | 0 | Standby Mode | | 1 | Normal Mode |	
12	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset (active low) after power is supplied	
13	SCA I2C	Serial data input / output pin in I2C interface operation. (CMDSEL=0). If use I2C interface, reserve 4.7Kohm resistance to IOVCC on FPC. If not use, please connect it to IOVCC.	
14	SCL I2C	Serial clock input in I2C interface. (CMDSEL=0) If use I2C interface, reserve 4.7Kohm resistance to IOVCC on FPC. If not use, please connect it to IOVCC	
15	NC	No connection	
16	IOVCC	Power supply	
17	IOVCC	Power supply	
18	IOVCC	Power supply	
19	GND	Ground	

20	D3P	LVDS Data differential signal input pins. (Data lane 3) if not used , Please connected to VSSH or open	
21	D3N	LVDS Data differential signal input pins. (Data lane 3) if not used , Please connected to VSSH or open	
22	GND	Ground	
23	CLKP	LVDS CLOCK differential signal input pins. if not used , Please connected to VSSH or open	
24	CLKN	LVDS CLOCK differential signal input pins. if not used , Please connected to VSSH or open	
25	GND	Ground	
26	D2P	LVDS Data differential signal input pins. (Data lane 2) if not used , Please connected to VSSH or open	
27	D2N	LVDS Data differential signal input pins. (Data lane 2) if not used , Please connected to VSSH or open	
28	GND	Ground	
29	D1P	LVDS Data differential signal input pins. (Data lane 1) if not used , Please connected to VSSH or open	
30	D1N	LVDS Data differential signal input pins. (Data lane 1) if not used , Please connected to VSSH or open	
31	GND	Ground	
32	D0P	LVDS Data differential signal input pins. (Data lane 0) if not used , Please connected to VSSH or .open	
33	D0N	LVDS Data differential signal input pins. (Data lane 0) if not used , Please connected to VSSH or .open	
34	GND	Ground	
35	NC	No connection	
36	VPP	External High voltage pin is used in OTP program mode, the power is operate at 7.8V.If not used, let them open	
37	GND	Ground	
38	GND	Ground	
39	GND	Ground	
40	NC	No connection	

BLU:

No.	Symbol	Function
1	LEDA1	Backlight anode
2	LEDA2	Backlight anode
3	LEDA3	Backlight anode
4	LEDK1	Backlight cathode
5	LEDK2	Backlight cathode
6	LEDK3	Backlight cathode

9. AC Characteristics

9.1. Reset Timing
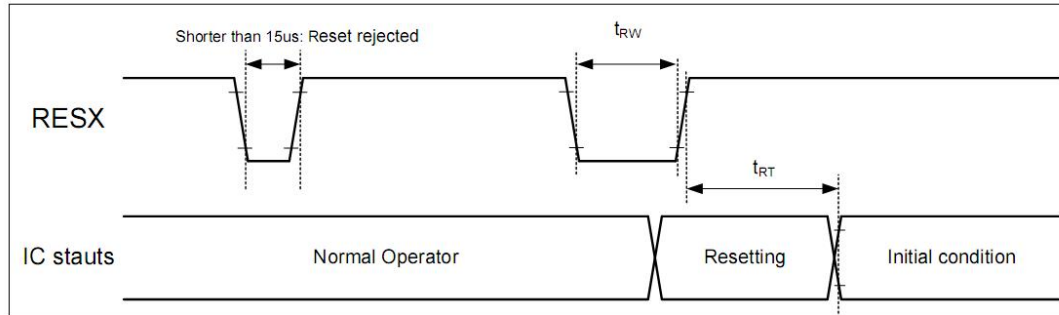
Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset "L" pulse width[2]	RESX	20	-	µs
t_{RT}	Reset complete time[3]	-	-	$5^{(5)}$	ms
		-	-	$120^{(6)\,(7)\,(8)}$	ms

Note:

(1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset complete time (t_{RT}) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 15 µs	Reset Rejected
Longer than 20 µs	Reset
Between 15 µs and 20 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:
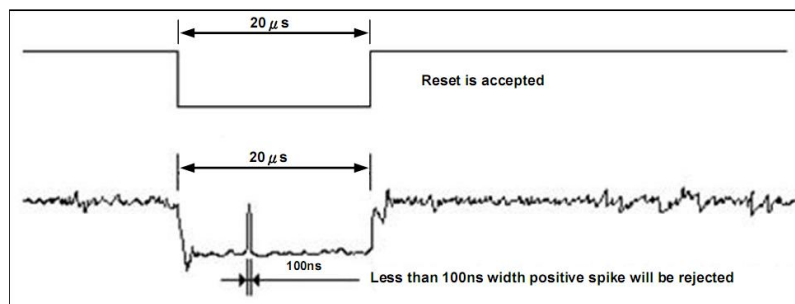
Reset timings

(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out command, it is necessary to wait 120msec then send RESX.

9.2. SPI electronic characteristics
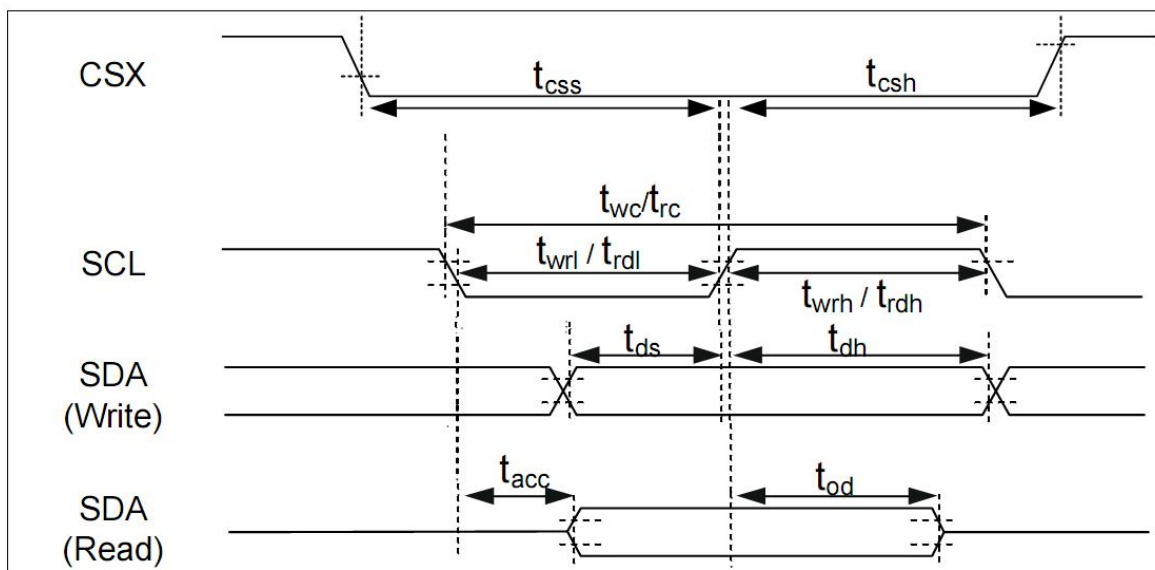
(T$_A$=25°C, IOVCC=3.3V, VCI=3.3V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{css} t_{csh}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
SCL (Write)	t_{wc} t_{wrh} t_{wrl}	Write cycle Control pulse "H" duration Control pulse "L" duration	100 40 40	- - -	ns	-
SCL (Read)	t_{rc} t_{rdh} t_{rdl}	Read cycle Control pulse "H" duration Control pulse "L" duration	150 60 60	- - -	ns	-
SDA (Write)	t_{ds} t_{dt}	Data setup time Data hold time	30 30	- -	ns	Note[1]
SDA (Read)	t_{acc} t_{od}	Read access time Output disable time	- 10	35 50	ns	

Note: (1) For maximum C$_L$=30pF, for minimum C$_L$=8pF.
     (2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
     (3) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

9.3. LVDS electronic characteristics

T_{SW}: Strobe width (Internal data sampling window)
R_{spos} : Receiver strobe position
T_{RSKM} : Receiver strobe margin
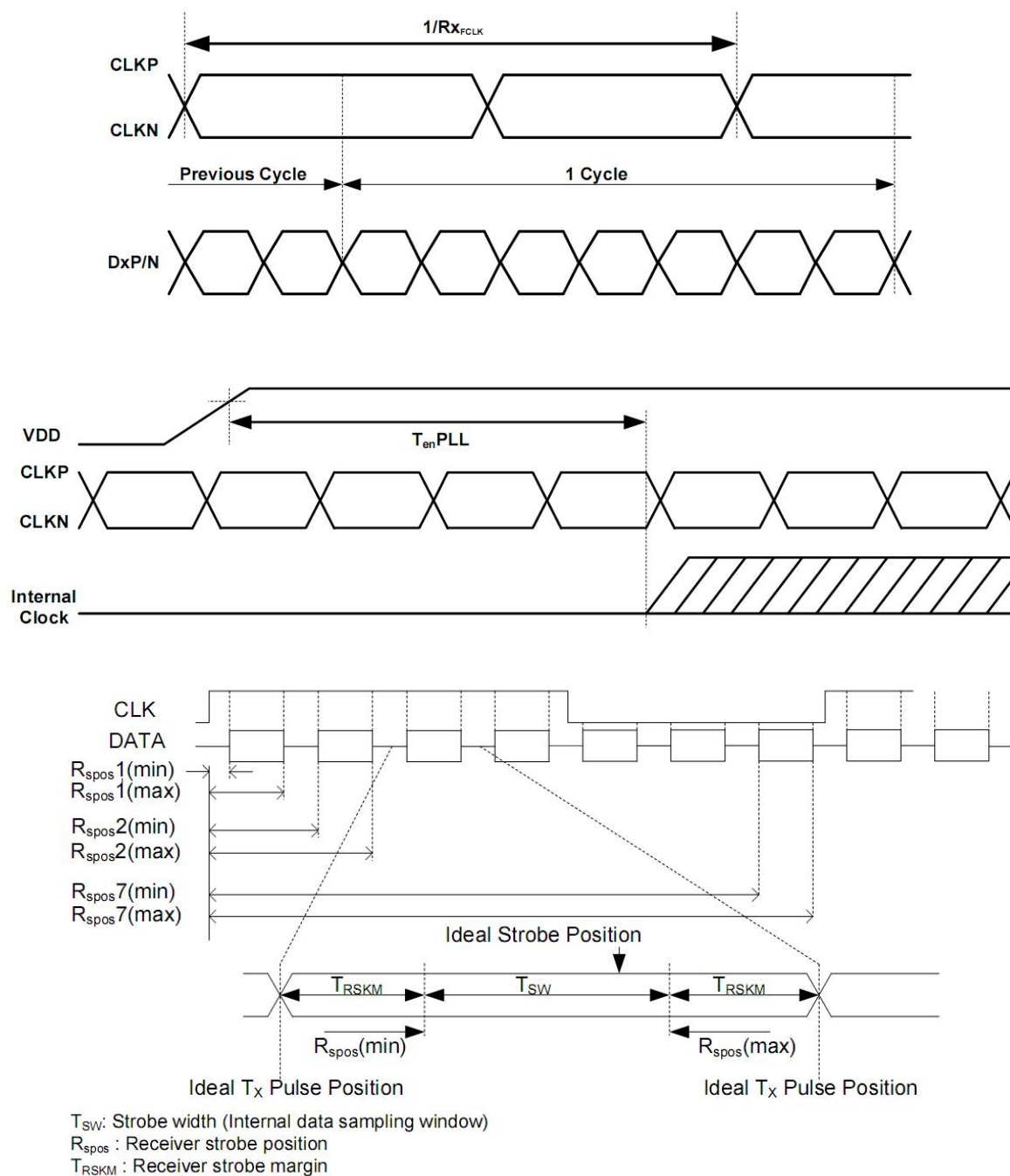
Signal	Symbol	Min.	Typ	Max.	Unit	Description
Clock frequency	Rx_{FCLK}	30	-	75	MHz	-
Input data skew margin	T_{RSKM}	500	-	-	ps	$|VID| = 200mV$ $RxVCM = 1.2V$ $@Rx_{FCLK}=75MHz$
Clock high time	T_{LVCH}	-	$4/(7\times Rx_{FCLK})$	-	ns	-
Clock low time	T_{LVCL}	-	$3/(7\times Rx_{FCLK})$	-	ns	-
PLL wake-up time	$T_{en}PLL$	-	-	150	us	-

9.4. LVDS Data format

1）6bit LVDS Input

2）8bit LVDS Input(VESA)

9.5. Timings for DSI Video mode

Vertical Timings

Horizontal Timings

RGB Timing Table :
TBD
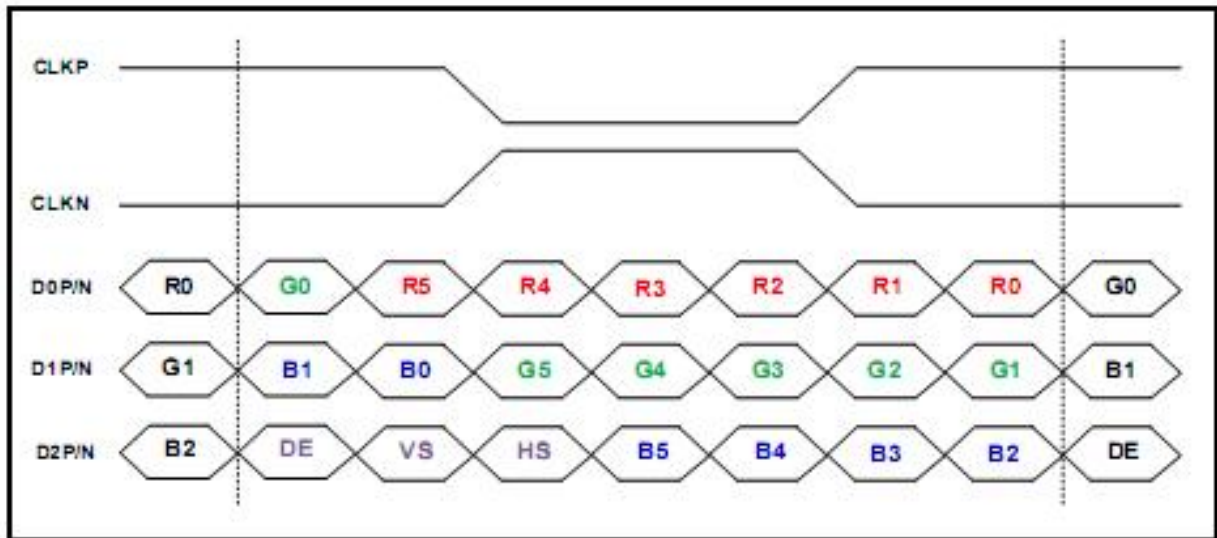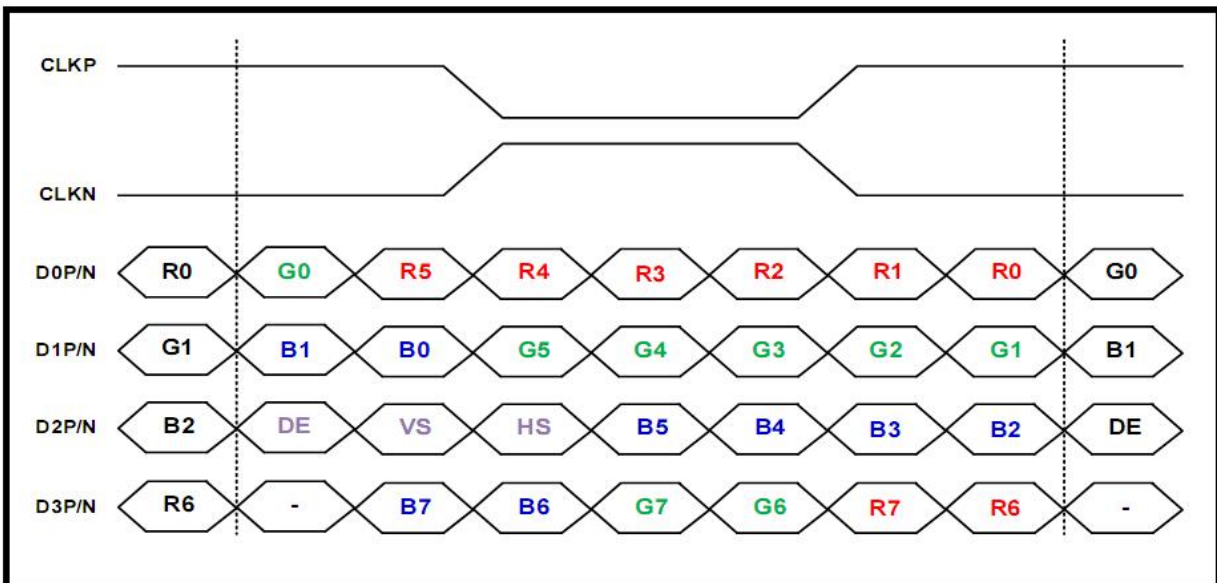
10. Quality Assurance

10.1. Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

10.2. Standard for Quality Test

10.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

10.2.2. Sampling Criteria:

Visual inspection: AQL 1.5

Electrical functional: AQL 0.65.

10.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

10.3. Nonconforming Analysis & Disposition

10.3.1.   Nonconforming analysis:

10.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

10.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

10.3.1.3. If cannot finish the analysis on time, customer will be notified with the progress status.

10.3.2. Disposition of nonconforming:

10.3.2.1. Non-conforming product over PPM level will be replaced.

10.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

10.4. Agreement Items

Shall negotiate with customer if the following situation occurs:

10.4.1. There is any discrepancy in standard of quality assurance.

10.4.2. Additional requirement to be added in product specification.

10.4.3. Any other special problem.

10.5. Standard of the Product Visual Inspection

10.5.1. Appearance inspection:

10.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

10.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

10.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,
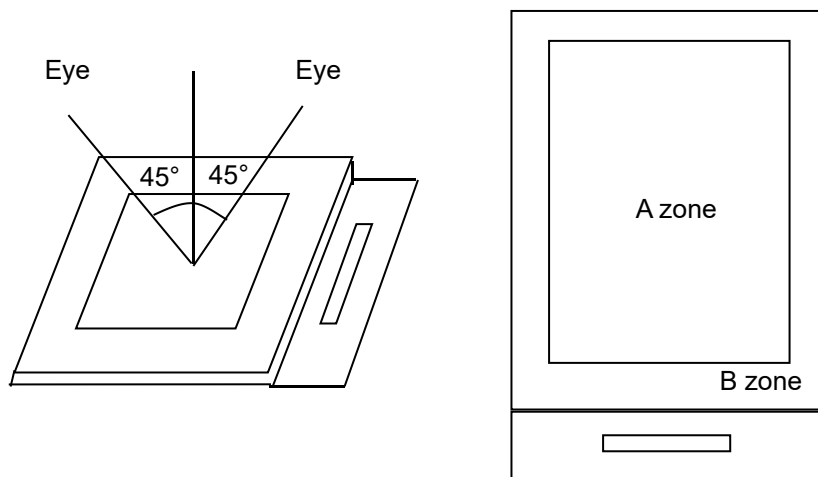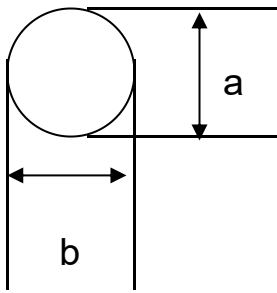
10.5.2. Basic principle:
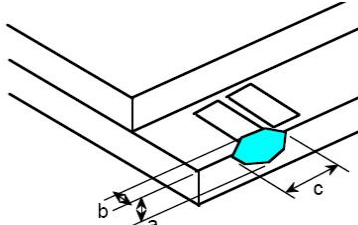
        10.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.
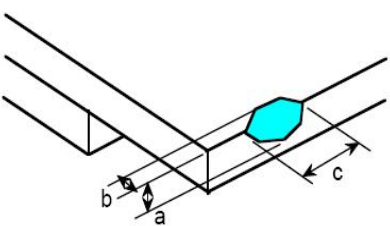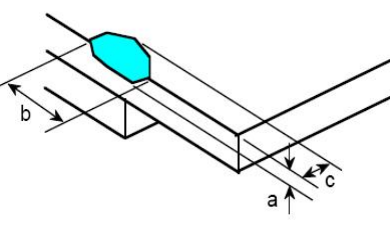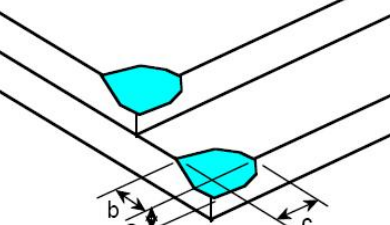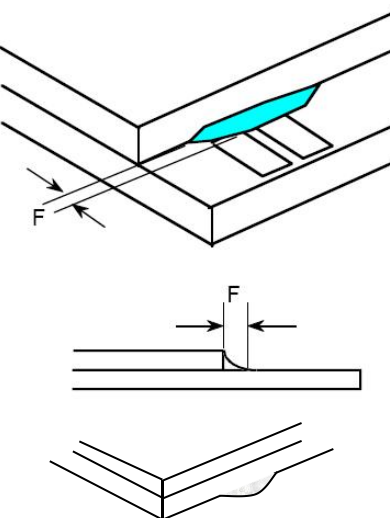
        10.5.2.2. New item must be added on time when it is necessary.

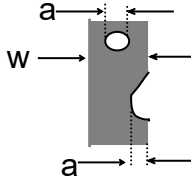## 10.6. Inspection Specification

No.	Item	Criteria (Unit: mm)		
01	Black / White spot Foreign material (Round type) Pinholes Stain Particles inside cell. (Minor defect)	 $\varphi = (a + b)/2$ Distance between 2 defects should more than 5mm apart.		

		Area / Size	Acc. Qty
		$\varphi \leq 0.20$	Ignore
		$0.20 < \varphi \leq 0.50$	N≤3
		$0.50 < \varphi$	0

No.	Item				
02	Electrical Defect (Minor defect)	**Bright dot**	Display Area	Total	Note1
			N≤2	N≤2	
		Dark dot	N≤4	N≤4	
		Total dot	N≤4	N≤4	
		Mura	**Not visible through 5% ND filters.**		Note 2

Remark:
1. Bright dot caused by scratch and foreign object accords to item 1.

| 03 | Black and White line Scratch Foreign material (Line type) (Minor defect) | |

Black and White line Scratch / Foreign material (Line type) (Minor defect):

Length	Width	Acc. Qty
/	W ≦ 0.1	Ignore
L ≦ 2.5	0.1 ＜ W ≦ 0.2	3
L＞2.5	0.2 ＜ W	0
Total		3

Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.

Glass Crack (Minor defect):

Crack is potential to enlarge, any type is not allowed.

Glass Chipping Pad Area: (Minor defect)

Length and Width	Acc. Qty
c > 3.0, b< 1.0	1
c< 3.0, b< 1.0	3
a<Glass Thickness	

06	Glass Chipping Rear of Pad Area: (Minor defect) 	<table><tr><th>Length and Width</th><th>Acc. Qty</th></tr><tr><td>c > 3.0, b< 1.0</td><td>1</td></tr><tr><td>c< 3.0, b< 1.0</td><td>2</td></tr><tr><td>c< 3.0, b< 0.5</td><td>4</td></tr><tr><td colspan="2">a<Glass Thickness</td></tr></table>
07	Glass Chipping Except Pad Area: (Minor defect) 	<table><tr><th>Length and Width</th><th>Acc. Qty</th></tr><tr><td>c > 3.0, b< 1.0</td><td>1</td></tr><tr><td>c< 3.0, b< 1.0</td><td>2</td></tr><tr><td>c< 3.0, b< 0.5</td><td>4</td></tr><tr><td colspan="2">a<Glass Thickness</td></tr></table>
08	Glass Corner Chipping: (Minor defect) 	<table><tr><th>Length and Width</th><th>Acc. Qty</th></tr><tr><td>c < 3.0, b< 3.0</td><td>Ignore</td></tr><tr><td colspan="2">a<Glass Thickness</td></tr></table>
09	Glass Burr: (Minor defect) 	<table><tr><th>Length</th><th>Acc. Qty</th></tr><tr><td>F < 1.0</td><td>Ignore</td></tr></table> Glass burr don't affect assemble and module dimension.

10	FPC Defect: (Minor defect) 	10.1 Dent, pinhole width a<w/3. (w: circuitry width.) 10.2 Open circuit is unacceptable. 10.3 No oxidation, contamination and distortion.
11	Bubble on Polarizer (Minor defect)	<table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.30</td><td>Ignore</td></tr><tr><td>0.30 <φ≤0.50</td><td>N≤2</td></tr><tr><td>0.50 < φ</td><td>N=0</td></tr></table>
12	Dent on Polarizer (Minor defect)	<table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.25</td><td>Ignore</td></tr><tr><td>0.25 <φ≤0.50</td><td>N≤4</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table>
13	Bezel	13.1 No rust, distortion on the Bezel. 13.2 No visible fingerprints, stains or other contamination.
14	PCB	14.1 No distortion or contamination on PCB terminals. 14.2 All components on PCB must same as documented on the BOM/component layout. 14.3 Follow IPC-A-600F.
15	Soldering	Follow IPC-A-610C standard
16	Electrical Defect (Major defect)	The below defects must be rejected. 16.1 Missing vertical / horizontal segment, 16.2 Abnormal Display. 16.3 No function or no display. 16.4 Current exceeds product specifications. 16.5 LCD viewing angle defect. 16.6 No Backlight. 16.7 Dark Backlight. 16.8 Touch Panel no function.

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

10.7. Classification of Defects

10.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

10.7.2. Two minor defects are equal to one major in lot sampling inspection.

10.8. Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.
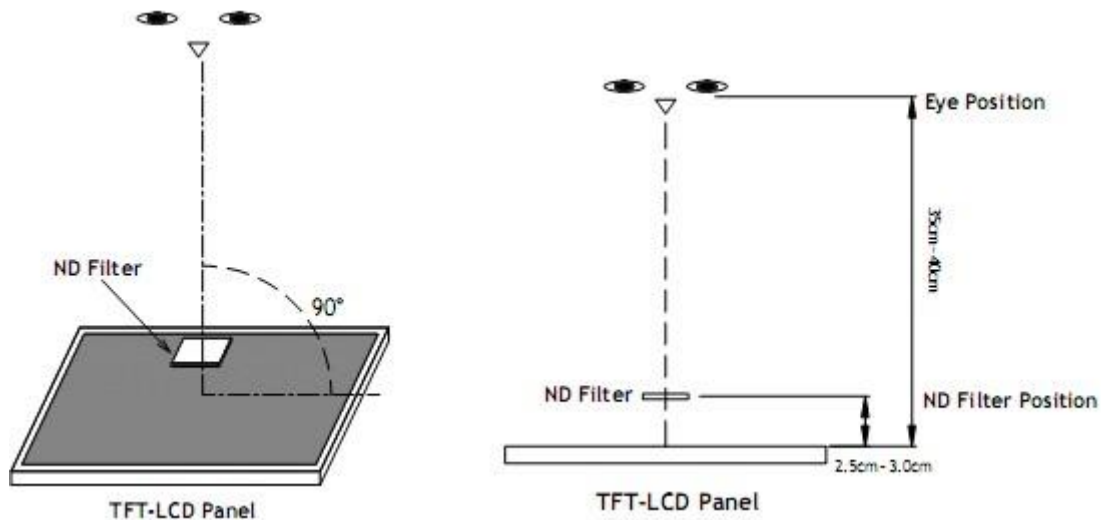
10.9. Packing

10.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

10.9.2. Modules inside package box should have compliant mark.

10.9.3. All direct package materials shall offer ESD protection.

Note1:Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.

Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

11. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	**70℃, 96Hrs**	2	GB/T2423.2 -2008
2	Low Temperature Operating	**-20℃, 96Hrs**	2	GB/T2423.1 -2008
3	High Humidity Storage	**50℃, 90%RH, 96Hrs**	2	GB/T2423.3 -2016
4	High Temperature Storage	**70℃, 96Hrs**	2	GB/T2423.2 -2008
5	Low Temperature Storage	**-20℃, 96Hrs**	2	GB/T2423.1 -2008
6	Thermal Cycling Test Storage	**-20℃, 30min~70℃, 30min, 20 cycles.**	2	GB/T2423.22 -2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X,Y,Z 30 min for each direction.	-	GB/T5170.14 -2009
8	Electrical Static Discharge	Air:±4KV 150pF/330Ω 5 times	2	GB/T17626.2 -2018
		Contact:±2KV 150pF/330Ω 5 times		
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	-	GB/T2423.7 -2018

Note1.　No defection cosmetic and operational function allowable.

Note2.　Total current Consumption should be below double of initial value

12. Precautions and Warranty

12.1. Safety

12.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

12.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

12.2. Handling

12.2.1. Reverse and use within ratings in order to keep performance and prevent damage.

12.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

12.3. Storage

12.3.1. Do not store the LCD module beyond the specified temperature ranges.

12.3.2. Strong light exposure causes degradation of polarizer and color filter.

12.4. Metal Pin (Apply to Products with Metal Pins)

12.4.1. Pins of LCD and Backlight

12.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

12.4.1.2. Recommended Soldering Conditions
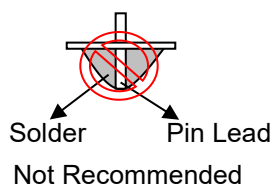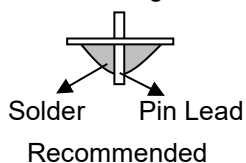
Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

12.4.1.3. Solder Wetting

Solder   Pin Lead   Solder   Pin Lead
Recommended   Not Recommended

12.4.2. Pins of EL

12.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

12.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

12.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm
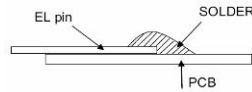
Recommended Solder Temperature: 270～290℃

Typical Soldering Time: ≤2s
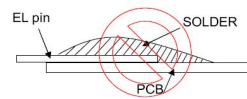
Minimum solder distance from EL lamp (body):2.0mm

12.4.2.4. No horizontal press on the EL leads during soldering.

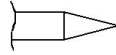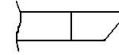12.4.2.5. 180° bend EL leads three times is not allowed.

12.4.2.6. Solder Wetting

| EL pin | SOLDER |
| PCB |

Recommended   Not Recommended

12.4.2.7. The type of the solder iron:
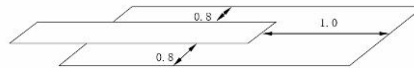
Recommended   Not Recommended

12.4.2.8. Solder Pad

0.8   1.0
0.8

12.5. Operation

12.5.1.　Do not drive LCD with DC voltage

12.5.2.　Response time will increase below lower temperature

12.5.3.　Display may change color with different temperature

12.5.4.　Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear "fractured".

12.5.5.　Do not connect or disconnect the LCM to or from the system when power is on.

12.5.6.　Never use the LCM under abnormal condition of high temperature and high humidity.

12.5.7.　Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

12.5.8.　Do not display the fixed pattern for long time（we suggest the time not longer than one hour）because it will develop image sticking due to the TFT structure.

12.6. Static Electricity

12.6.1.　CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

12.6.2.　The normal static prevention measures should be observed for work clothes and benches.

12.6.3.　The module should be kept into anti-static bags or other containers resistant to static for storage.

12.7. Limited Warranty

12.7.1.　Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

12.7.2.　If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

12.7.3.　After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

13. Packaging

TBD

14. Outline Drawing