PRODUCT SPECIFICATION

3.12” OLED Display Module
MODEL: YDP OLED W 312

ROHS

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY
TFT X. B 20221216	TFT S. G. H 20221216	TFT 周福云 20221216	TFT L. Q 20221216

knitter-switch

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2022.08.01	ZFY	Initial Release	
1.1	2022.12.16	LQ	Add Weight	P4

Table of Contents

1. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	3.12”	
Resolution	256 x 64	Pixels
Module Outline	88 (H) x 27.8 (V) x 2(T) (Note1)	mm
Active Area	76.78(H) x 19.18(V)	mm
Pixel Size	300 (H) x 300 (V)	um
Interface	8-bit 80XX-series Parallel Interface 8-bit 68XX-series Parallel Interface 4-SPI Interface 3-SPI Interface	
With or without touch panel	Without	
Driver IC	SSD1322UR1(COF)	-
Display color	white	
Weight	11	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	VCC	-0.5	21	V	1,2
	VDD	-0.5	2.75	V	1,2
	VDDIO	-0.5	VCI	V	1,2
	VCI	-0.3	4	V	1,2
Operating Temperature	T_{OP}	-40	85	°C	
Storage Temperature	T_{STG}	-65	150	°C	3
Life Time (100 cd/m^2)		20000	-	hour	4
Life Time (90 cd/m^2)		25000	-	hour	4
Life Time (80 cd/m^2)		30000	-	hour	4

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

Note 4: VCC= 12V, Ta= 25°C, 50% Checkerboard.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Interface Pins Definition

<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>NC</td><td>Reserved Pin. (The N.C. pins between function pins are reserved for compatible and flexible design.)</td></tr>
<tr><td>2</td><td>VSS</td><td>Ground pin.</td></tr>
<tr><td>3</td><td>VCC</td><td>Power supply for panel driving voltage.</td></tr>
<tr><td>4</td><td>VCOMH</td><td>Voltage Output High Level for COM Signal.</td></tr>
<tr><td>5</td><td>VLSS</td><td>Analog system ground pin.</td></tr>
<tr><td>6</td><td>D7</td><td rowspan="8">Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.</td></tr>
<tr><td>7</td><td>D6</td></tr>
<tr><td>8</td><td>D5</td></tr>
<tr><td>9</td><td>D4</td></tr>
<tr><td>10</td><td>D3</td></tr>
<tr><td>11</td><td>D2</td></tr>
<tr><td>12</td><td>D1</td></tr>
<tr><td>13</td><td>D0</td></tr>
<tr><td>14</td><td>E/RD</td><td>Read/Write Enable or Read</td></tr>
<tr><td>15</td><td>R/W</td><td>Read/Write Select or Write</td></tr>
<tr><td>16
17</td><td>BS0
BS1</td><td>Communicating Protocol Select
<table>
<tr><th></th><th>BS0</th><th>BS1</th></tr>
<tr><td>3-SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 80XX parallel</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 68XX parallel</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>18</td><td>DC</td><td>Data/Command Control</td></tr>
<tr><td>19</td><td>CS</td><td>Chip Select</td></tr>
<tr><td>20</td><td>RES</td><td>Power Reset for Controller and Driver</td></tr>
<tr><td>21</td><td>FR</td><td>This pin is No Connection pins. Nothing should be connected to this pin. This pin should be left open individually.</td></tr>
<tr><td>22</td><td>IREF</td><td>Current Reference for Brightness Adjustment</td></tr>
<tr><td>23</td><td>NC</td><td>Reserved Pin. (The N.C. pins between function pins are reserved for compatible and flexible design.)</td></tr>
<tr><td>24</td><td>VDDIO</td><td>Power supply for interface logic level</td></tr>
<tr><td>25</td><td>VDD</td><td>Power supply pin for core logic operation.</td></tr>
<tr><td>26</td><td>VCI</td><td>Low voltage power supply</td></tr>
<tr><td>27</td><td>VSL</td><td>This is segment voltage reference pin. When external VSL is used, connect with resistor and diode to ground (details depend on application).</td></tr>
<tr><td>28</td><td>VLSS</td><td>Analog system ground pin.</td></tr>
<tr><td>29</td><td>VCC</td><td>Power supply for panel driving voltage</td></tr>
<tr><td>30</td><td>NC</td><td>Reserved Pin. (The N.C. pins between function pins are reserved for compatible and flexible design.)</td></tr>
</table>

4. Optics & Electrical Characteristics

4.1. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Luminance	Lbr		60	80	-	cd/m2
C.I.E. (White)	(x)	C.I.E. 1931	0.25	0.29	0.33	
	(y)		0.27	0.31	0.35	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			160	-	-	degree

4.2. DC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage for OLED	VCC	11.5	12.	12.5	V
Logic Supply Voltage	VDD	2.4	2.5	2.6	V
Supply voltage for Operation	VCI	2.4	2.8	3.5	V
Power Supply for I/O pins	VDDIO	1.65		VCI	V
Operating Current for VCI	ICI	-	95	120	μA
Operating Current for VCC	ICC	-	34.5	40	mA
High Level Input	VIH	0.8×VDDIO	-	VDDIO	V
Low Level Input	VIL	0	-	0.2× VDDIO	V
High Level Output	VOH	0.9×VDDIO	-	VDDIO	V
Low Level Output	VOL	0	-	0.1×VDDIO	V

4.3. INTERFACE TIMING CHART

4.3.1. 8080-Series MCU Parallel Interface Timing Characteristics

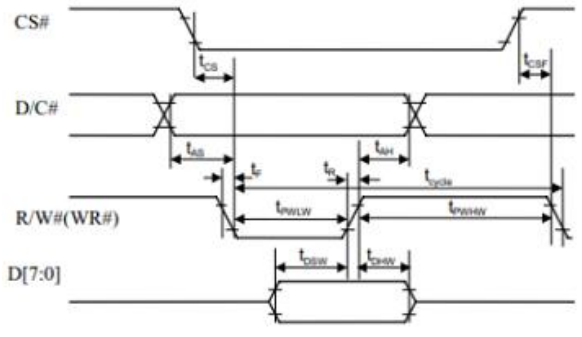
(V_{DDIO}-V_{SS} = 1.65V-2.1V, V_{CI} - V_{SS} = 2.4V-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	220	ns
t_{PWLR}	Read Low Time	200	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

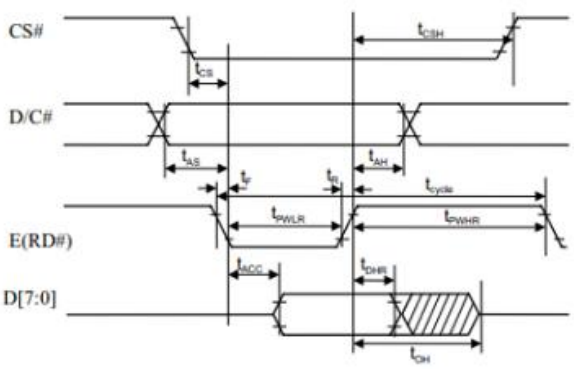
(V_{DDIO}-V_{SS} = 2.1V-V_{CI} , V_{CI} - V_{SS} = 2.4V-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	300 100	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Write cycle



Read cycle



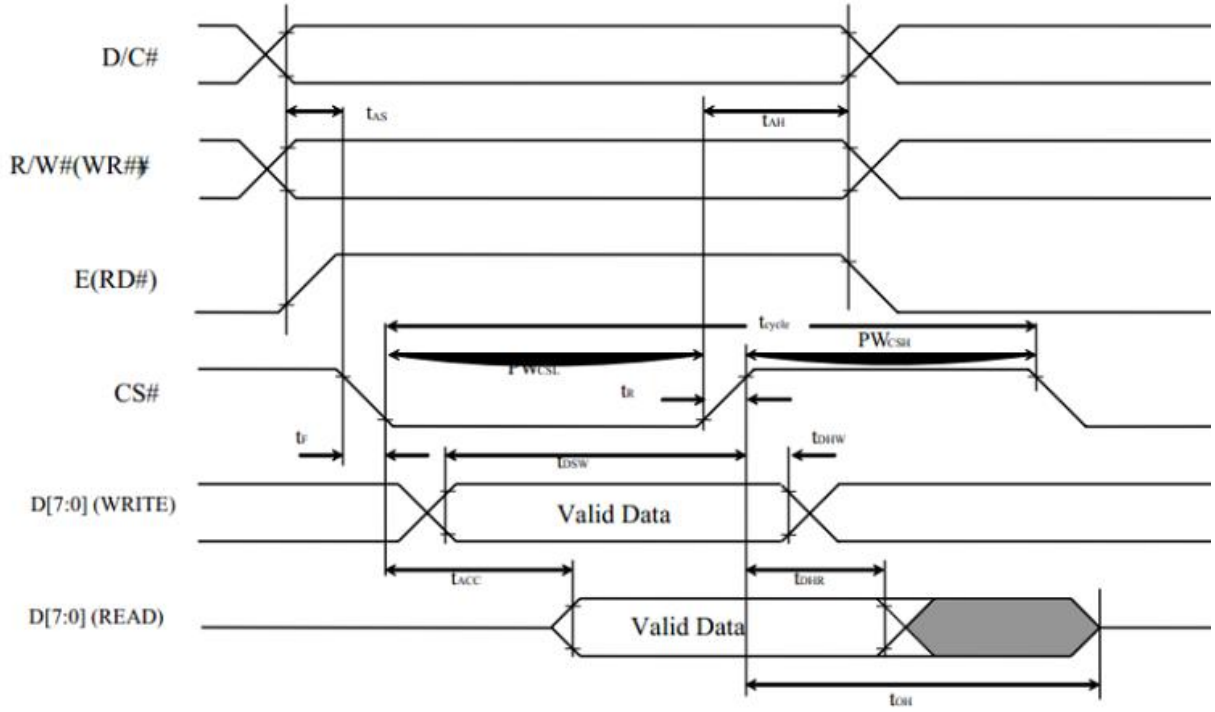
4.3.2. 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DDIO} -V_{SS} = 1.65V-2.1V, V_{CI} - V_{SS} = 2.4V-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	200	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	450 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

(V_{DDIO} -V_{SS} = 2.1V-V_{CI} , V_{CI} - V_{SS} = 2.4V-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	300 100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	150 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns


D/C#
R/W#(WR#)
E(RD#)
CS#
D[7:0] (WRITE)
D[7:0] (READ)
tAS
tAH
tcycle
PWCSH
PWCSL
tR
tF
tDHW
tDSW
Valid Data
tACC
tDHR
Valid Data
tOH

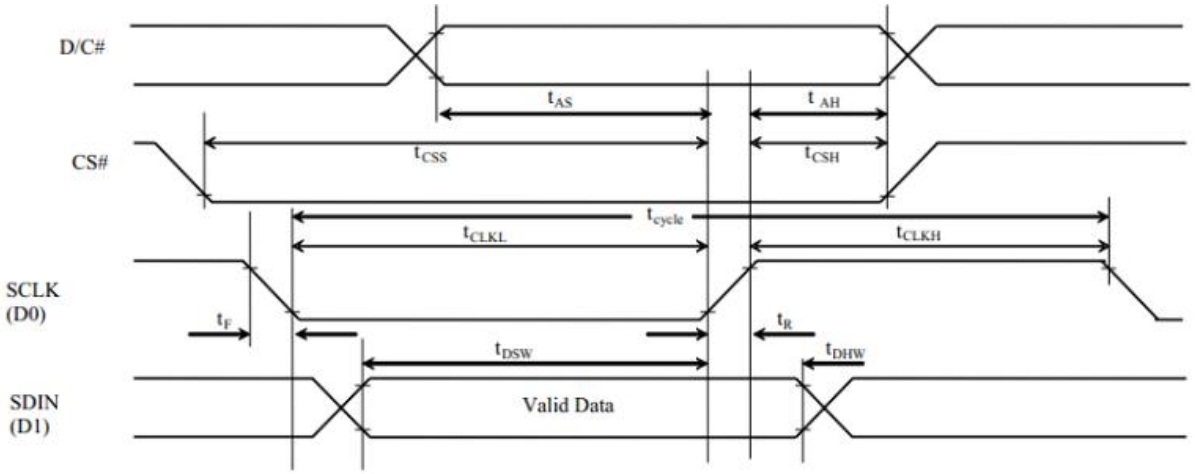
4.3.3. Serial Interface Timing Characteristics: (4-wire SPI)

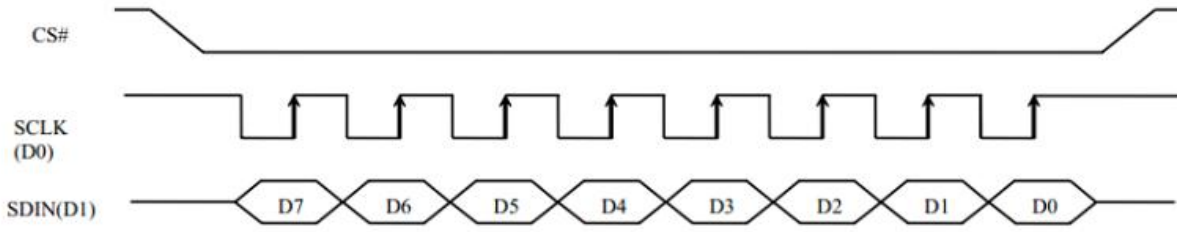
(V_{DDIO}-V_{SS} = 1.65V-2.1V, V_{CI} - V_{SS} = 2.4V-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	35	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	40	-	-	ns
t_{CLKH}	Clock High Time	40	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

(V_{DDIO}-V_{SS} = 2.1V-V_{CI} , V_{CI} - V_{SS} = 2.4V-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	25	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	25	-	-	ns
t_{CLKH}	Clock High Time	40	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns





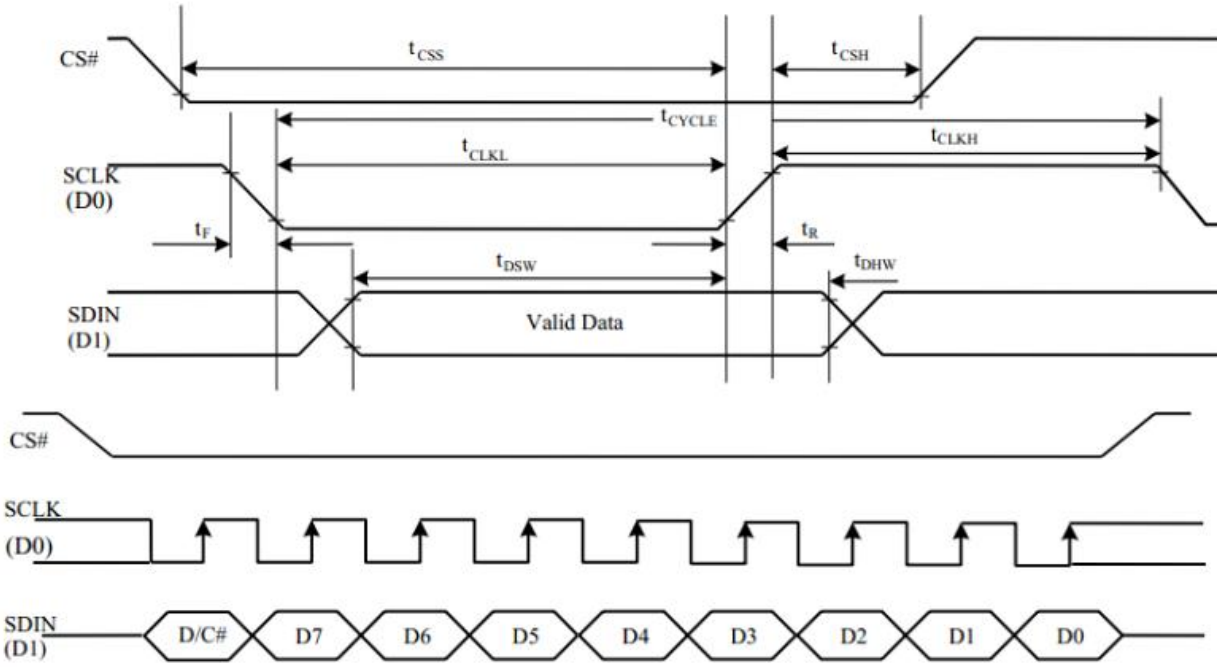
4.3.4. Serial Interface Timing Characteristics: (3-wire SPI)

(V_{DDIO} -V_{SS} = 1.65V-2.1V, V_{CI} - V_{SS} = 2.4V-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	35	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	40	-	-	ns
t_{CLKH}	Clock High Time	25	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

(V_{DDIO} -V_{SS} = 2.1V-V_{CI} , V_{CI} - V_{SS} = 2.4V-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	25	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	25	-	-	ns
t_{CLKH}	Clock High Time	25	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



5. Outgoing Quality Control Specifications

5.1. Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature: 23 ± 5°C

Humidity: 55 ± 15% RH

Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥ 50cm

Distance between the Panel & Eyes of the Inspector: ≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

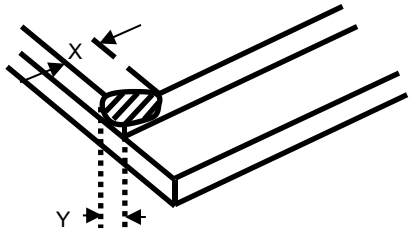
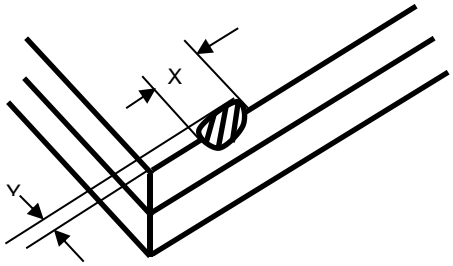
5.2. Sampling Plan

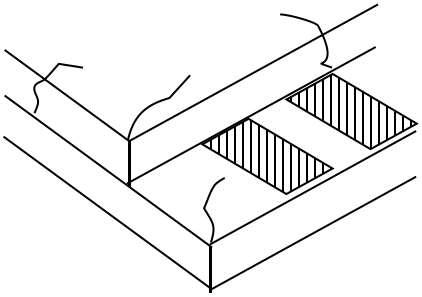
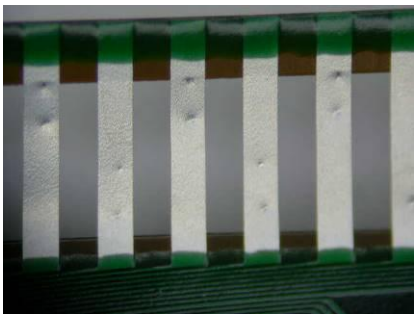
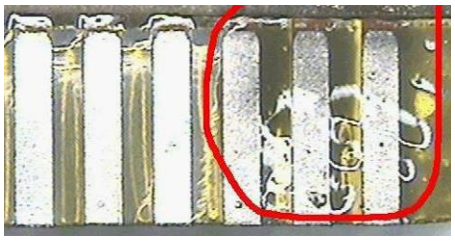
Level II, Normal Inspection, Single Sampling, MIL-STD-105E

5.3. Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

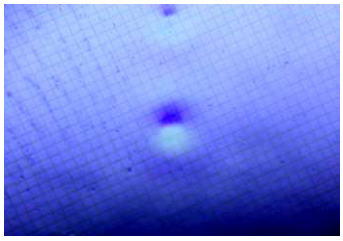
5.3.1. Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)  

Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

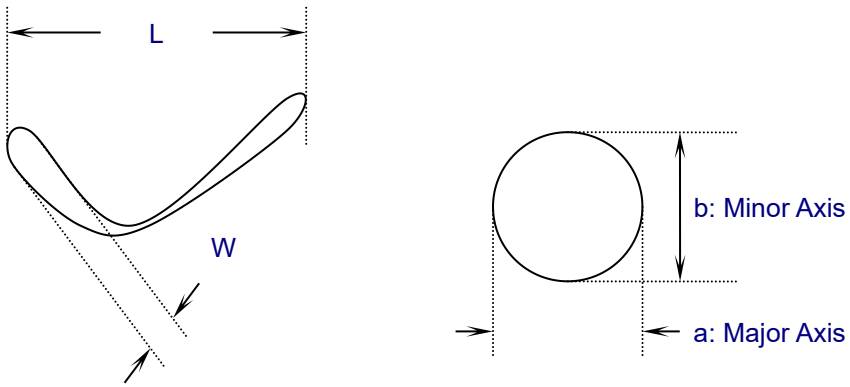
5.3.2. Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

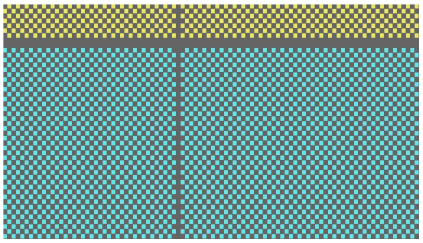
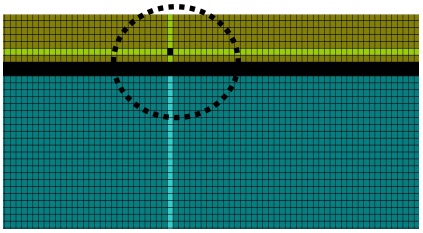
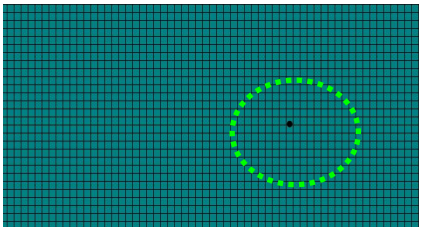
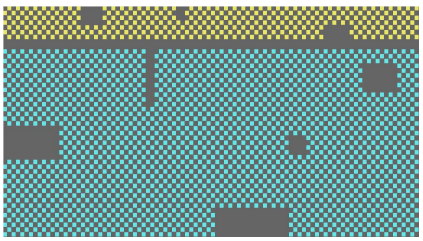
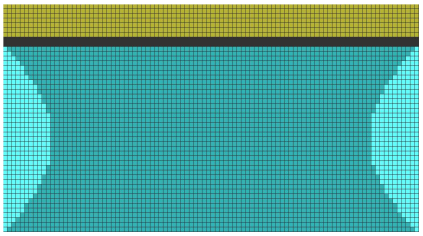
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

Note 1：Protective film should not be tear off when cosmetic check.

Note 2：Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



5.3.3. Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

6. Reliability Specification

6.1. Contents of Reliability Tests

No	Item	Condition	Quantity
1	High Temperature Operating	**70℃, 240Hrs**	2
2	Low Temperature Operating	**-40℃, 240Hrs**	2
3	High Humidity	**60℃, 90%RH, 120Hrs**	2
4	High Temperature Storage	**85℃, 240Hrs**	2
5	Low Temperature Storage	**-40℃, 240Hrs**	2
6	Thermal Cycling Test	**-40℃, 30min ~ 85℃, 30min, 24 cycles.**	2

Note1. The samples used for the above tests do not include polarizer.

Note2. No moisture condensation is observed during tests.

6.2. Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5℃; 55±15% RH.

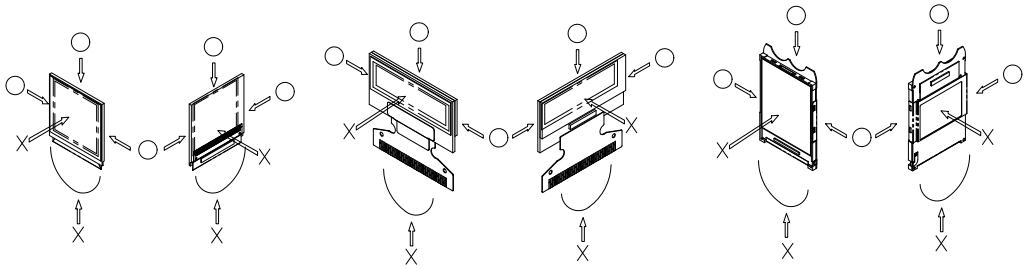
7. Precautions When Using These OLED Display Modules

7.1. Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OLED display module very carefully when placing OLED display module into the system housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OLED display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OLED display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OLED display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the

protection film before assembling it. At this time, if the OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

7.2. Storage Precautions

1) When storing OLED display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0 ° C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Newvision technology Co.,Ltd.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

7.3. Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OLED display module, fasten the external plastic housing section.
7) If power supply to the OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1316

   *Connection (contact) to any other potential than the above may lead to rupture of the IC.

7.4. Precautions when disposing of the OLED display modules

Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

7.5. Other Precautions

1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.
4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

7.6. Warranty

The warranty period shall last twelve months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve months. We shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

8. Outline Drawing