PRODUCT SPECIFICATION

1.29” OLED Display Module
MODEL: YDP OLED W 129

ROHS

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY

knitter-switch

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2019.07.02	ZDT	Initial Release	

Table of Contents

1. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	1.29”	
Display Mode	Passive Matrix	
Resolution	128 x 64	Pixels
Module Outline	32.42 (H) x 21.36 (V) x 1.427 (T) (Note1)	mm
Active Area	29.42(H) x 14.7(V)	mm
Pixel Size	230(H) x 230(V)	um
Display Colors	Monochrome (White)	
Interface	8-bit 68XX/80XX Parallel 4-wire SPI IIC	
With or without touch panel	Without	
Driver IC	SSD1315	-
Weight	TBD	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4.0	V	1,2
Supply Voltage for Display	V_{CC}	0	16.5	V	1,2
Supply Voltage for DC/DC	VBAT	-0.3	4.5	V	1, 2
Operating Temperature	T_{OP}	-40	85	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (120 cd/m^2)		10,000	-	hour	4
Life Time (80 cd/m^2)		24,000	-	hour	4
Life Time (60 cd/m^2)		32,000	-	hour	4

Note 1: All the above voltages are on the basis of “V_{SS} = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 4. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 9.0V, T_a = 25°C, 50% Checkerboard.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Interface Pins Definition

<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>N.C.(GND)</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.</td></tr>
<tr><td>2</td><td>C2P</td><td>Positive Terminal of the Flying Inverting Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>3</td><td>C2N</td><td>Negative Terminal of the Flying Boost Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>4</td><td>C1P</td><td>Positive Terminal of the Flying Inverting Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>5</td><td>C1N</td><td>Negative Terminal of the Flying Boost Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>6</td><td>VBAT</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.</td></tr>
<tr><td>7</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>8</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>9</td><td>VDD</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>10</td><td>NC</td><td>Reserved Pin
The N.C. pin between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>11</td><td>BS1</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS1</th><th>BS2</th></tr>
<tr><td>I^2C</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>12</td><td>BS2</td></tr>
</table>

13	CS#	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
14	RES#	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
15	D/C#	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
16	R/W#	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
17	E/RD#	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
18	D0	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.
19	D1	
20	D2	
21	D3	
22	D4	
23	D5	
24	D6	
25	D7	

26	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5μA maximum.
27	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
28	VCC	Power Supply for OLED Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
29	NC	Reserved Pin The N.C. pin between function pins are reserved for compatible and flexible design.
30	N.C.(GND)	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

4. Optics & Electrical Characteristics

4.1. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (VCC Supplied Externally)	Lbr	Note 5	60	-	-	cd/m2
Brightness (VCC Generated by Internal DC/DC)	Lbr	Note 5	60	80	-	cd/m2
C.I.E. (White)	(x)	C.I.E. 1931	0.25	0.29	0.33	
	(y)		0.27	0.31	0.35	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			-	Free	-	degree

Optical measurement taken at VDD = 2.8V, VCC = 9V & 7.25V.

4.2. DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	VCC	Note 5 (Internal DC/DC Disable)	8.5	9.0	9.5	V
Supply Voltage for DC/DC	VBAT	Internal DC/DC Enable	3.6	-	4.5	V
Supply Voltage for Display (Generated by Internal DC/DC)	VCC	Note 5 (Internal DC/DC Enable)	7.0	-	7.5	V
High Level Input	VIH	IOUT = 100μA, 3.3MHz	0.8×VDD	-	VDD	V
Low Level Input	VIL	IOUT = 100μA, 3.3MHz	0	-	0.2×VDD	V
High Level Output	VOH	IOUT = 100μA, 3.3MHz	0.9×VDD	-	VDD	V
Low Level Output	VOL	IOUT = 100μA, 3.3MHz	0	-	0.1×VDD	V
Operating Current for VDD	IDD		-	180	300	μA
Operating Current for VCC (VCC Supplied Externally)	ICC	Note 6	-	21	28	mA
Operating Current for VBAT (VCC Generated by Internal DC/DC)	IBAT	Note 7	-	44	46	mA
Sleep Mode Current for VDD	IDD, SLEEP		-	-	10	μA
Sleep Mode Current for VCC	ICC, SLEEP		-	-	10	μA

Note 5 : Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer’s request.

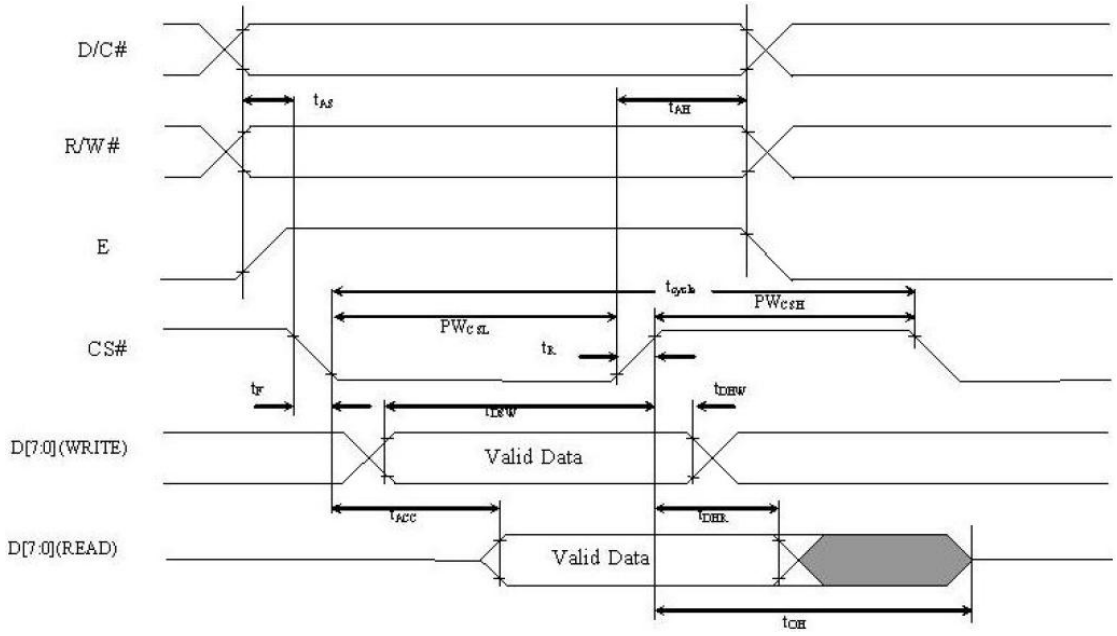
Note 6: VDD = 2.8V, VCC = 9V, 100% Display Area Turn on.

Note 7: VDD = 2.8V, VCC = 7.25V, 100% Display Area Turn on.

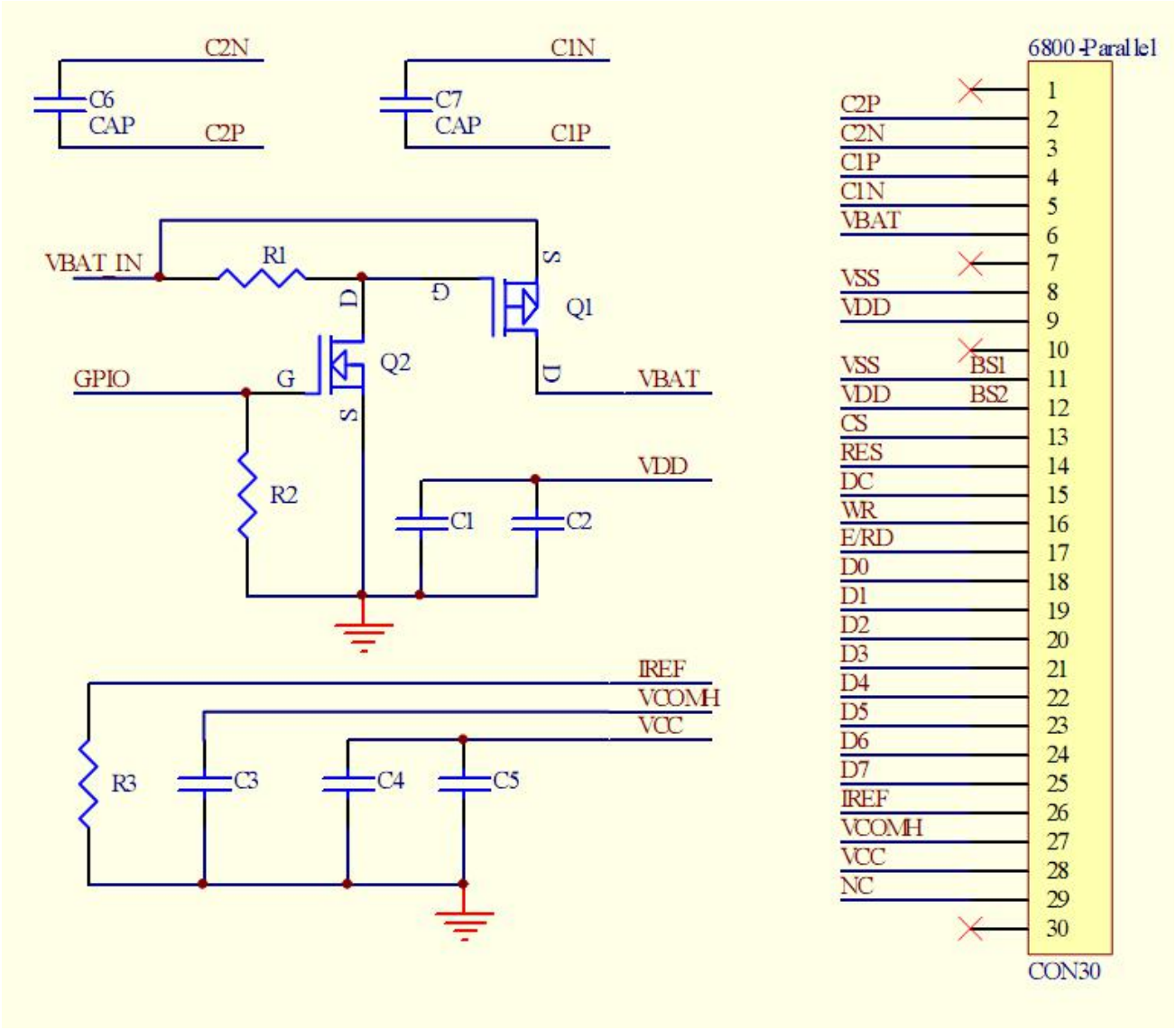
4.3. AC Characteristics

4.3.1. 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	5	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	180	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	180	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns



4.3.2. 68XX-Series MPU Parallel Interface with Internal Charge Pump



Recommended Components:

C1: 0.1μF / 6.3V, X5R C2: 4.7μF / 6.3V, X5R C3: 2.2Mf/16v

C4: 4.7μF / 16V, X7R C5: 0.1μF / 16V, X7R

C6,C7: 1μF / 16V, X7R

R3: 620kΩ, R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ Q1: FDN338P Q2: FDN335N

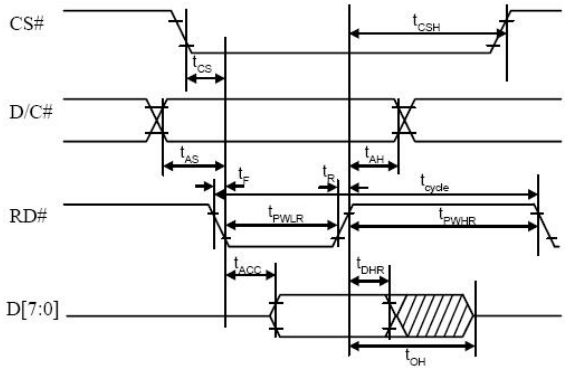
Notes:

VDD: 1.65~3.5V, it should be equal to MPU I/O voltage. Vin: 3.6~4.5V

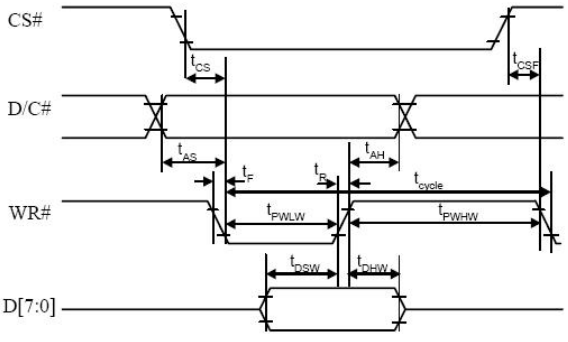
VBAT will be connected to VDD when VCC be connected to external source (12V), R3 should be replaced as 910 kΩ.

4.3.3. 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	180	ns
t_{PWLR}	Read Low Time	180	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

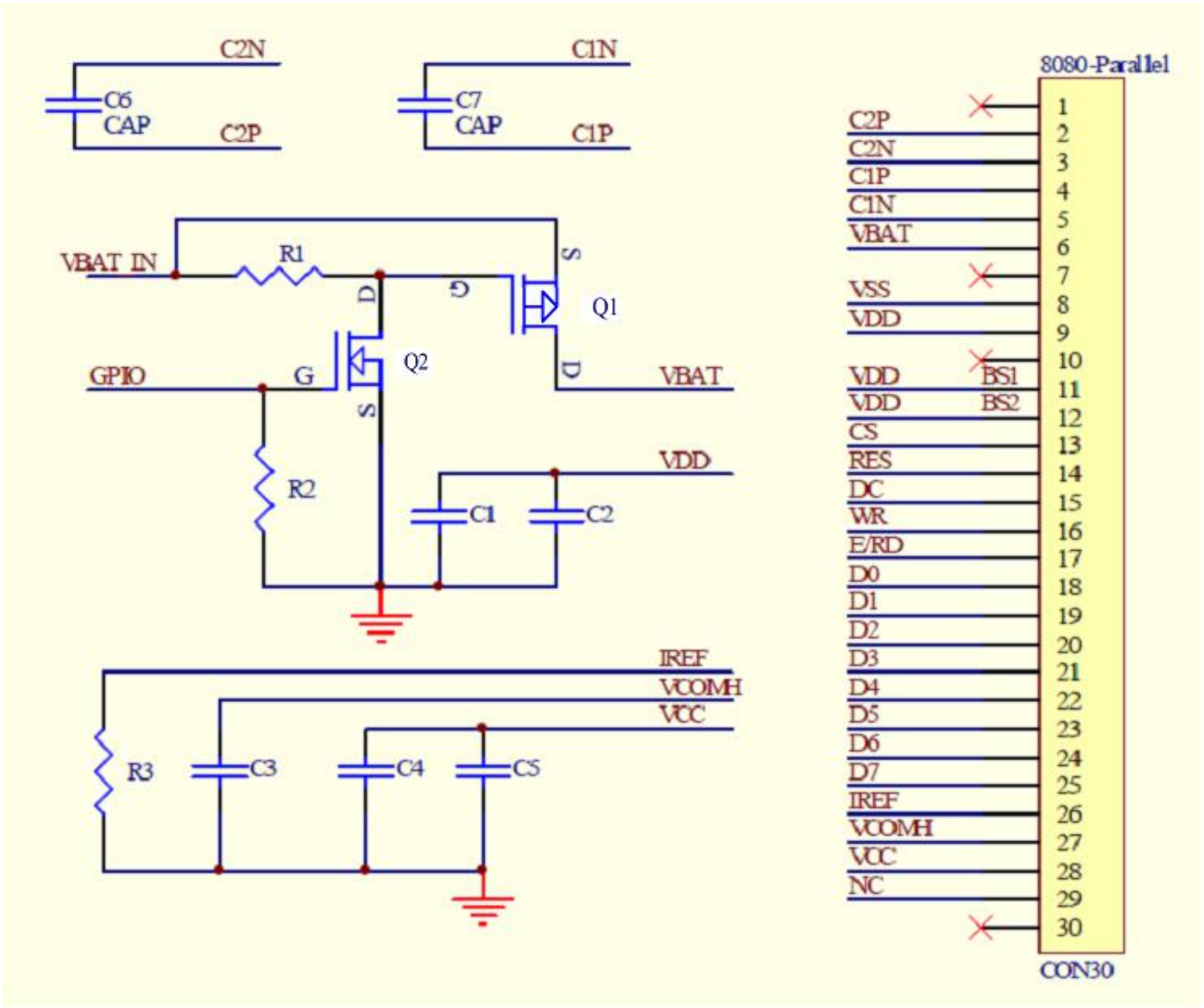


(Read Timing)



(Write Timing)

4.3.4. 80XX-Series MPU Parallel Interface with Internal Charge Pump



Recommended Components:

C1: 0.1μF / 6.3V, X5R C2: 4.7μF / 6.3V, X5R C3: 2.2Mf/16v

C4: 4.7μF / 16V, X7R C5: 0.1μF / 16V, X7R

C6,C7: 1μF / 16V, X7R

R3: 910kΩ, R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ Q1: FDN338P Q2: FDN335N

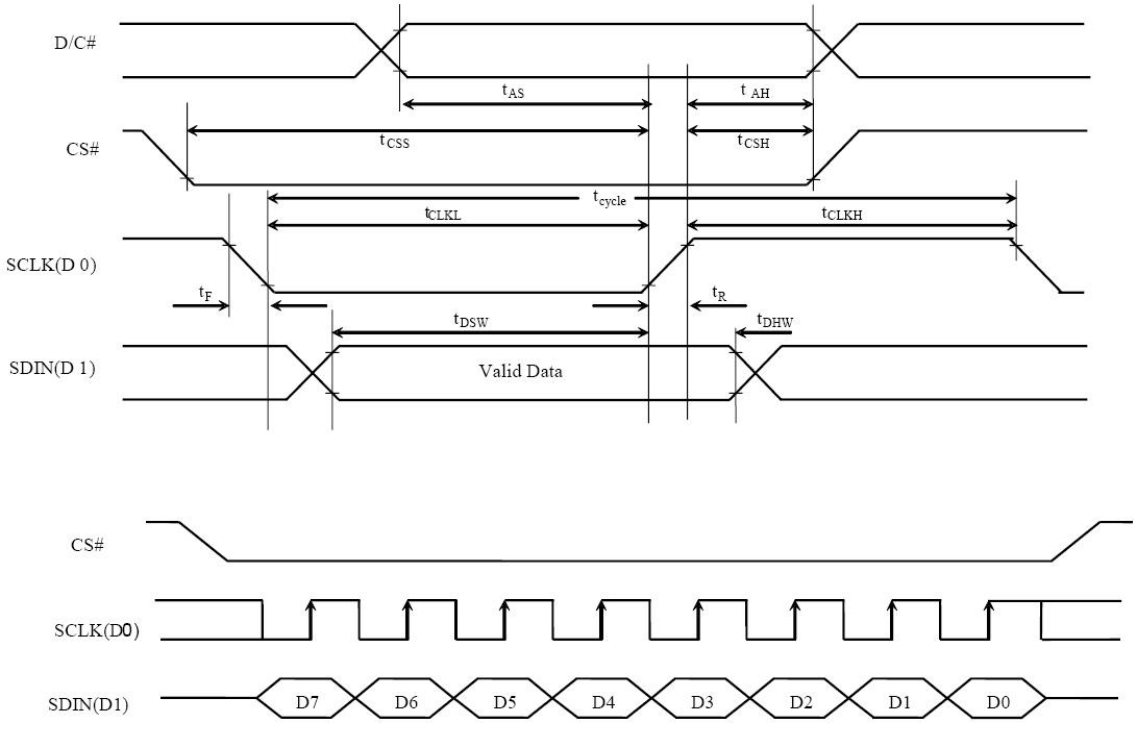
Notes:

VDD: 1.65~3.5V, it should be equal to MPU I/O voltage. Vin: 3.6~4.5V

VBAT will be connected to VDD when VCC be connected to external source (12V), R3 should be replaced as 910 kΩ.

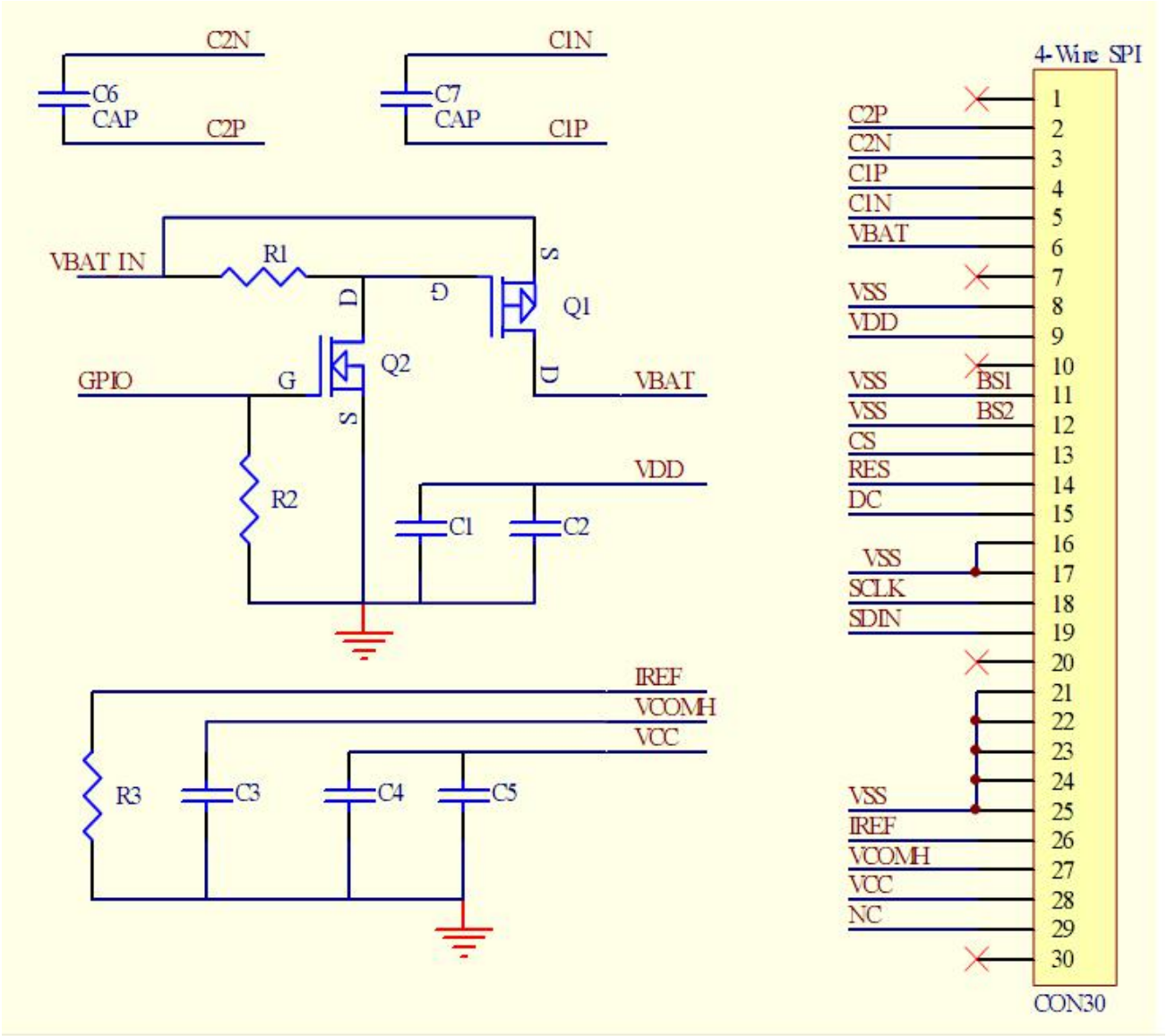
4.3.5. Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	25	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	30	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns



4.3.6. 4-wire Serial Interface with Internal Charge Pump

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1: 0.1μF / 6.3V, X5R C2: 4.7μF / 6.3V, X5R C3: 2.2Mf/16v

C4: 4.7μF / 16V, X7R C5: 0.1μF / 16V, X7R

C6,C7: 1μF / 16V, X7R

R3: 910kΩ, R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ Q1: FDN338P Q2: FDN335N

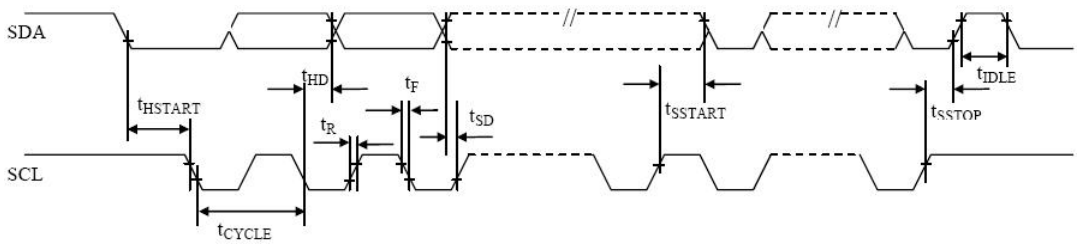
Notes:

VDD: 1.65~3.5V, it should be equal to MPU I/O voltage. Vin: 3.6~4.5V

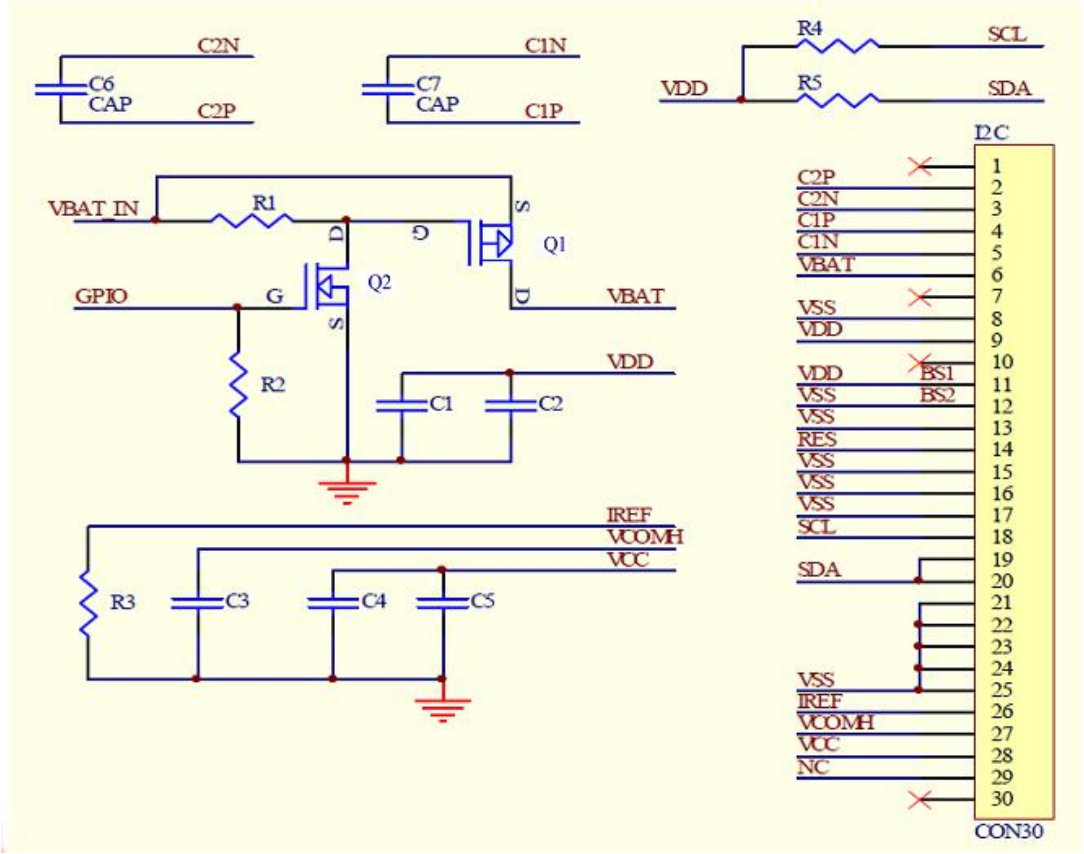
VBAT will be connected to VDD when VCC be connected to external source (12V), R3 should be replaced as 910 kΩ.

4.3.7. IIC Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs



4.3.8. IIC Interface with Internal Charge Pump



Recommended Components:

C1: 0.1μF / 6.3V, X5R C2: 4.7μF / 6.3V, X5R C3: 2.2Mf/16v

C4: 4.7μF / 16V, X7R C5: 0.1μF / 16V, X7R

C6,C7: 1μF / 16V, X7R

R3: 910kΩ, R3 = (Voltage at IREF - VSS) / IREF

R1, R2: 47kΩ R4, R5: 4.7kΩ Q1: FDN338P Q2: FDN335N

Notes:

VDD: 1.65~3.5V, it should be equal to MPU I/O voltage. Vin: 3.6~4.5V

VBAT will be connected to VDD when VCC be connected to external source (12V), R3 should be replaced as 910 kΩ.

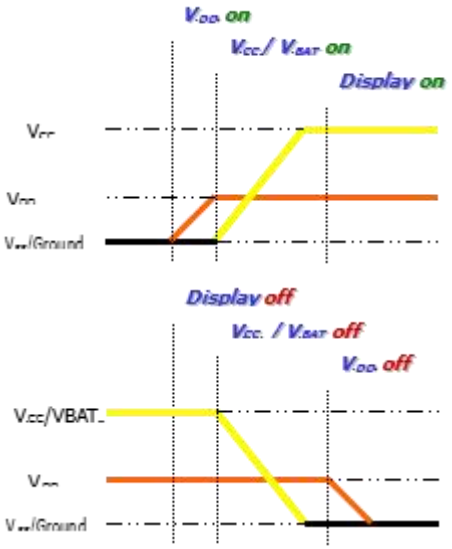
5. Functional Specification

5.1. Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OLED panel enough time to complete the action of charge and discharge before/after the operation.

5.1.1. Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}/ V_{BAT}
6. Delay 100ms (When V_{CC} is stable)
7. Send Display on command



5.1.2. Power down Sequence:

1. Send Display off command
2. Power down V_{CC} / V_{BAT}
3. Delay 100ms

(When V_{CC} / V_{BAT} is reach 0 and panel is completely discharges)

4. Power down V_{DD}

Note:

1) Since an ESD protection circuit is connected between VDD and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.

2) VCC / VBAT should be kept float (disable) when it is OFF.

3) Power Pins (VDD, VCC, VBAT) can never be pulled to ground under any circumstance.

4) VDD should not be power down before VCC / VBAT power down.

5.2. Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1.Display is OFF

2.12864 Display Mode

3.Normal segment and display data column and row address mapping

(SEG0 mapped to column address 00h and COM0 mapped to row address 00h)

4.Shift register data clear in serial interface

5.Display start line is set at display RAM address 0

6.Column address counter is set at 0

7.Normal scan direction of the COM outputs

8.Contrast control register is set at 7Fh

9.Normal display mode (Equivalent to A4h command)

6. Outgoing Quality Control Specifications

6.1. Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

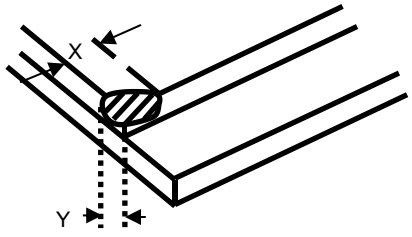
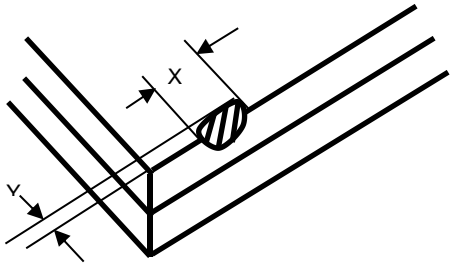
6.2. Sampling Plan

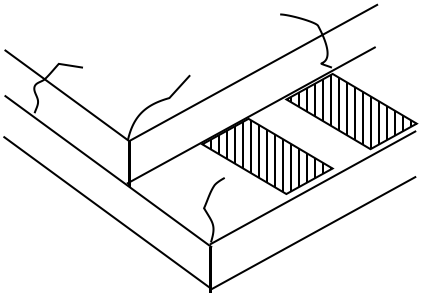
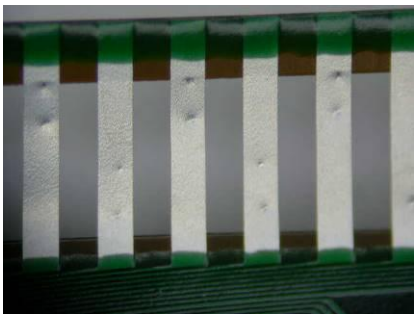
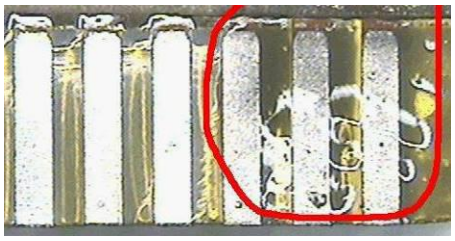
Level II, Normal Inspection, Single Sampling, MIL-STD-105E

6.3. Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

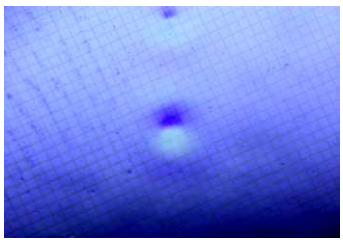
6.3.1. Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)  

Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

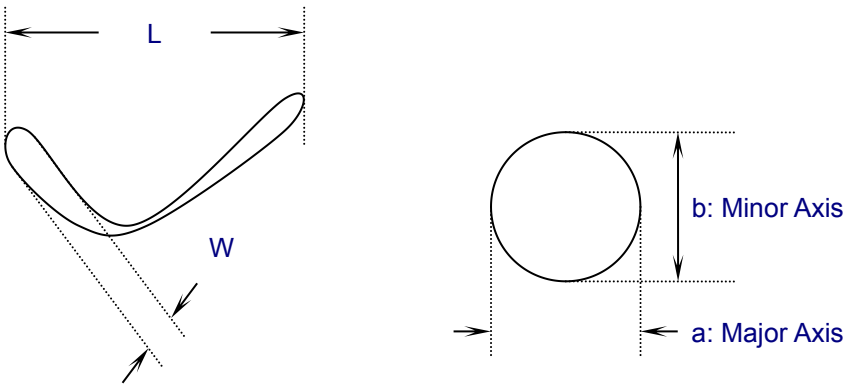
6.3.2. Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

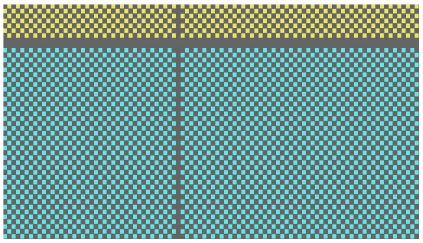
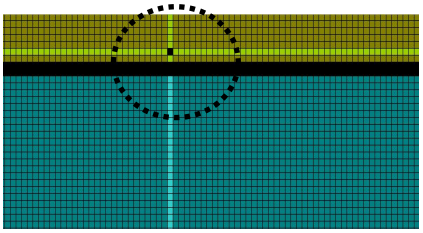
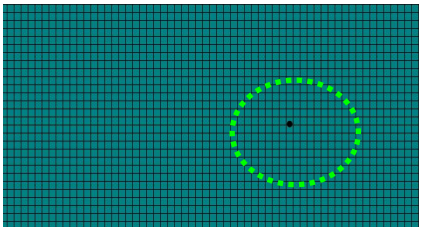
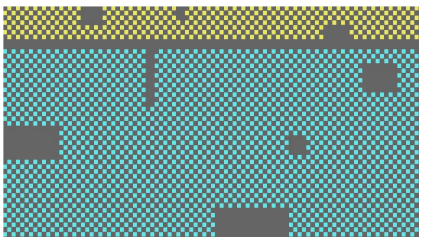
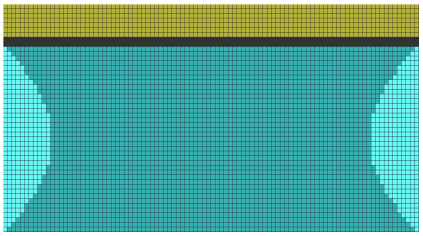
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

Note 1：Protective film should not be tear off when cosmetic check.

Note 2：Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3. Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Reliability Specification

7.1. Contents of Reliability Tests

No	Item	Condition	Criteria
1	High Temperature Operating	**70℃, 240Hrs**	The operational functions work.
2	Low Temperature Operating	**-40℃, 240Hrs**	
3	High Humidity	**60℃, 90%RH, 120Hrs**	
4	High Temperature Storage	**85℃, 240Hrs**	
5	Low Temperature Storage	**-40℃, 240Hrs**	
6	Thermal Cycling Test	**-40℃, 60min~85℃, 60min, 24 cycles.**	

Note1. The samples used for the above tests do not include polarizer.

Note2. No moisture condensation is observed during tests.

7.2. Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5℃; 55±15% RH.

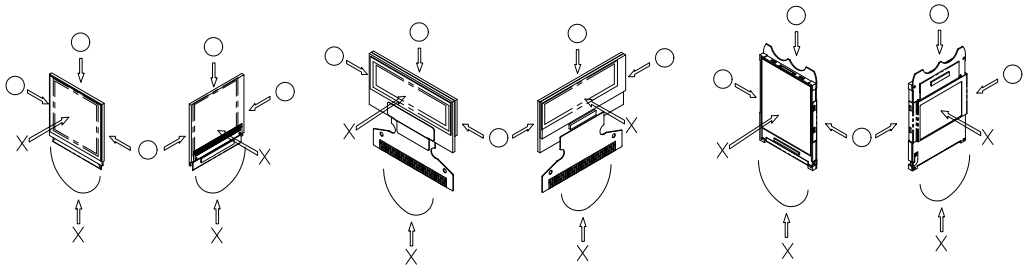
8. Precautions When Using These OLED Display Modules

8.1. Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OLED display module very carefully when placing OLED display module into the system housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OLED display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OLED display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OLED display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the

protection film before assembling it. At this time, if the OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2. Storage Precautions

1) When storing OLED display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0 ° C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Newvision technology Co.,Ltd.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3. Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OLED display module, fasten the external plastic housing section.
7) If power supply to the OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1316

   *Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4. Precautions when disposing of the OLED display modules

Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5. Other Precautions

1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.
4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

8.6. Warranty

The warranty period shall last twelve months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve months. We shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

9. Outline Drawing