

PRODUCT SPECIFICATION

OED 1.54[″] EPD MODULE MODEL: YDP EI 154 S Ver: 1.1

- < <>> Preliminary Specification
- < <> Finally Specification

	CUSTOMER'S APPROVAL						
CUSTOMER :							
SIGNATURE: DATE:							

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Revision History

Date	Originator	Detail	Remarks
2020.10.29	ZJW	Initial Release	
		Modify Module Parameter	P4
		Modify DC Characteristics	P5
2023.10.27	LQ	Modify Optical Characteristics	P5
		Modify Interface Timing Description	P8-11
		Modify Outline Drawing	P16
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1. General Description

The Product is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 1.54" active area contains 200x200 pixels, and has 2-bit full display capabilities. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	1.54"	
LCD type	AM EPD	
Resolution	200 x 200	Pixels
Module Outline	31.8(H) x 37.32 (V) x 1.0(T) (Note1)	mm
Active Area	27(H) x 27(V)	mm
Pixel Pitch	135(H) x 135(V)	um
Pixel Arrangement	Square	
Interface	3/4 LINE SPI	
With or Without Touch Panel	Without	
Operating Temperature	0~50	°C
Storage Temperature	-25~70	°C
Weight	2.18	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

Vss=0V, Ta=25°C

			- 00	
ltem	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	-0.5	4.0	V
Storage temperature	T _{STG}	-25	+70	°C
Operating temperature	Тор	0	+50	°C

Note 1: If Ta below 50°C, the maximal humidity is 90%RH, if Ta over 50°C, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10° C, and the back ground will become darker at high temperature operating.

4. DC Characteristics

ltem	Symbol	Min.	Тур.	Max.	Unit
Analogr supply Voltage	VDD	2.4	3.0	3.6	V
Logic Low input voltage	VIL	-	-	0.2*VDD	V
Logic High input voltage	Vih	0.8*VDD	-	-	V
Logic Low output voltage	Vol	0	-	0.1*VDD	V
Logic High output voltage	Vон	0.9*VDD	-	-	V
Typical operating current	loo	-	1.5	-	mA

5. Optical Characteristics

5.1. Optical Characteristics

					Ta=2	5°C, VDD	=3.0V
Symbol	Parameter	Conditions		Values			Notes
Symbol		Conditions	Min.	Тур.	Max	Units	notes
R	White Reflectivity	White	30	35	-	%	5-1
CR	Contrast Ratio		8:1	-	-	-	5-2
White∆L 24h	Reduce		-	≤4	-	-	-
T _{update}	Image update time	at 25 °C	-	3	-	Sec	-

Notes: 5-1. Luminance meter: Eye-One Pro Spectrophotometer.

5-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

6. Block Diagram and Power Supply



Driver PCBA

7. Interface Pins Definition

No.	Symbol	Function	Remark
1	NC	Do not connect with other NC pins	
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	Do not connect with other NC pins	
5	VDHR	Positive Source driving voltage 1	
6	TSCL	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I ² C Interface to digital temperature sensor Data pin	
8	BS	Bus Interface selection pin	Note 7-4
9	BUSYN	Busy state output pin	Note 7-3
10	RSTN	Reset signal input. Active Low.	
11	D/C	Data /Command control pin	Note 7-2
12	CSB	Chip select input pin	Note 7-1
13	SCL	Serial Clock pin (SPI)	
14	SDA	Serial Data pin (SPI)	
15	VDD	Power Supply for interface logic pins	
16	VDD	Power Supply for the chip	
17	VSS	Ground	
		Core logic power pin	
18	VDDD	VDDD can be regulated internally from VDD. A capacitor should be	
		connected between VDDD and VSS under all circumstances	
19	VPP	Power Supply for OTP Programming	
20	VSH	Positive Source driving voltage 2	
21	VGH	Positive Gate driving voltage	
22	VSL	Negative Source driving voltage	
23	VGL	Negative Gate driving voltage	
24	VCOM	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin Note 7-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

- Note 7-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.
- Note 7-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin High when
 - Outputting display waveform
 - Programming with OTP
 - Communicating with digital temperature sensor
- Note 7-4: Bus interface selection pin

BS1 State	MCU Interface					
L	4-lines serial peripheral interface(SPI)					
Н	3- lines serial peripheral interface(SPI) - 9 bits SPI					

8. MCU Interface

1) The module can support 3-wire/4-wire serial peripheral.MCU interface is pin selectable by BS1 shown in Table 8-1.

MCU Interface	Pin Name						
	BS1	RES#	CS#	D/C#	SCL	SDA	
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA	
3-wire serial peripheral interface (SPI) – 9 bits SPI	Н	RES#	CS#	L	SCL	SDA	

Table 8-1:Interface pins assignment under different MCU interface

Note:L is connected to Vss and H is connected to VDD.

8.1. MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C#and CS#. The write procedure 4-wire SPI is shown in Table 8-2

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	î	Data bit	Н	L

Table 8-2: Control pins status of 4-wire SPI

Note:

(1) L is connected to VSS and H is connected to VDD

(2) † stands for rising edge of signal

(3) SDA(Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7,D6,...DO. The level of D/C#should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according

to D/C# pin.



Write procedure in 4-wire SPI mode

In the read operation (Command 0x1B,0x27,0x2D,0x2E,0x2F,0x35). After CS# is pulled low,the first byte sent is command byte,D/C#is pulled low.After command byte sent,the following byte(s)read are data byte(s),so D/C#bit is then pulled high.An 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7,D6,to DO bit. Figure 6-2 shows the read procedure in 4-wire SPI.



Read procedure in 4-wire SPI mode

8.2. MCU Serial Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C#pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 8-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C#bit,D7 bit,D6 bit to DO bit. The first bit is D/C#bit which determines the following byte is command or data. When D/C#bit is 0, the following byte is command. When D/C#bit is 1, the following byte is data.

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	Î	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

8-3:Control pins status of 3-wire SPI

Note:

(4) L is connected to VSS and H is connected to VDD

(5) † stands for rising edge of signal



Write procedure in 3-wire SPI

In the read operation (Register 0x1B,0x27,0x2D,Ox2E,Ox2F,0x35).SDA data are transferred in the unit of 9 bits. After CS#pull low, the first byte is command byte, the D/C#bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C#bit is 1. After D/C#bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7,D6, to Do bit. Figure 8-4 shows the read procedure in 3-wire SPI.



8-4:Read procedure in 3-wire SPI mode

8.3. Serial Peripheral Interface

Symbol	Parameter	Min	Тур	Max	Unit
fscl	SCL frequency (Write Mode)	-	-	20	MHz
tcssu	Time CS# has to be low before the first rising edge of SCLK	60	-	-	ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	65	-	-	ns
tсянісн	Time CS# has to remain high between two transfers	100		-	ns
tsclhigh	Part of the clock period where SCL has to remain high	25	-	-	ns
tscllow	Part of the clock period where SCL has to remain low	25	-	-	ns
tsisu	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10	-	-	ns
tsihld	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40	-	-	ns
Read m	ode				
	ode Parameter	Min	Тур	Max	Unit
		Min -	Тур	Max 2.5	Unit MHz
Symbol	Parameter		-		
Symbol fscL	Parameter SCL frequency (Read Mode)	-	-	2.5	MHz
Symbol fscL tcssu tcsHLD	Parameter SCL frequency (Read Mode) Time CS# has to be low before the first rising edge of SCLK	- 100	-	2.5	MHz ns
Symbol fscL tcssU tcsHLD tcsHIGH	Parameter SCL frequency (Read Mode) Time CS# has to be low before the first rising edge of SCLK Time CS# has to remain low after the last falling edge of SCLK	- 100 50	•	2.5	MHz ns ns
Symbol fscL tcssu tcshLD tcshIGH tscLHIGH	Parameter SCL frequency (Read Mode) Time CS# has to be low before the first rising edge of SCLK Time CS# has to remain low after the last falling edge of SCLK Time CS# has to remain high between two transfers	- 100 50 250	· · ·	2.5	MHz ns ns ns
Symbol fscL tcssu	Parameter SCL frequency (Read Mode) Time CS# has to be low before the first rising edge of SCLK Time CS# has to remain low after the last falling edge of SCLK Time CS# has to remain high between two transfers Part of the clock period where SCL has to remain high	- 100 50 250 180	· · ·	2.5 - - -	MHz ns ns ns ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Serial Peripheral Interface Timing Characteristics



SPI timing diagram

8.4. Operation Flow and Code Sequence

General operation flow to drive display panel



9. Reliability Specification

No	Item	Condition	Quantity	y Criteria	
1	High Temperature Operating	50℃, 96Hrs	2	IEC 60 068-2-2Bp	
2	Low Temperature Operating	0℃, 96Hrs	2	IEC 60 068-2-2Ab	
3	ligh Humidity Storage 60°C, 80%RH, 96Hrs		2	IEC 60 068-2-3CA	
4	High Temperature Storage	70℃, 96Hrs	2	IEC 60 068-2-2Bp	
5	Low Temperature Storage	-25℃, 96Hrs	2	IEC 60 068-2-1 Ab	
6	Thermal Cycling Test Storage	-25℃, 30min~70℃, 30min, 50 cycles.	2	IEC 60 068-2-14	
7	Packing vibration	Frequency range:10Hz~500Hz Acceleration of gravity:1.04G X, Y, Z 60 min for each direction.	-	Full packed for shipment	
8	Drop Test (Packaged)	Height:122 cm,1 corner, 3 edges, 6 surfaces.		IEC 62179, IEC 62180	

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value.

10. Precautions and Warranty

10.1.Safety

- 10.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.
- 10.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

10.2. Handling

- 10.2.1. Reverse and use within ratings in order to keep performance and prevent damage.
- 10.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

10.3. Storage

- 10.3.1. Do not store the LCD module beyond the specified temperature ranges.
- 10.3.2. Strong light exposure causes degradation of polarizer and color filter.

10.4. Metal Pin (Apply to Products with Metal Pins)

- 10.4.1. Pins of LCD and Backlight
 - 10.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering
 - 10.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

Maximum Solder Temperature: 370°C

Maximum Solder Time: 3s at the maximum temperature

Recommended Soldering Temp: 350±20°C

Typical Soldering Time: ≤3s

10.4.1.3. Solder Wetting





10.4.2. Pins of EL

- 10.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.
- 10.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.
- 10.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270~290°C

Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

- 10.4.2.4. No horizontal press on the EL leads during soldering.
- $10.4.2.5,\,180^\circ$ bend EL leads three times is not allowed.

10.4.2.6. Solder Wetting



10.5.Operation

- 10.5.1. Do not drive LCD with DC voltage
- 10.5.2. Response time will increase below lower temperature
- 10.5.3. Display may change color with different temperature
- 10.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear "fractured".
- 10.5.5. Do not connect or disconnect the LCM to or from the system when power is on.
- 10.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.
- 10.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- 10.5.8. Do not display the fixed pattern for long time (we suggest the time not longer than one hour) because it will develop image sticking due to the TFT structure.

10.6.Static Electricity

- 10.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.
- 10.6.2. The normal static prevention measures should be observed for work clothes and benches.
- 10.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

10.7.Limited Warranty

- 10.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.
- 10.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.
- 10.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

11. Packaging

TBD